


Quanta Project Name: XM2

Dell Project Name: Reebok

X02(ST) Stage

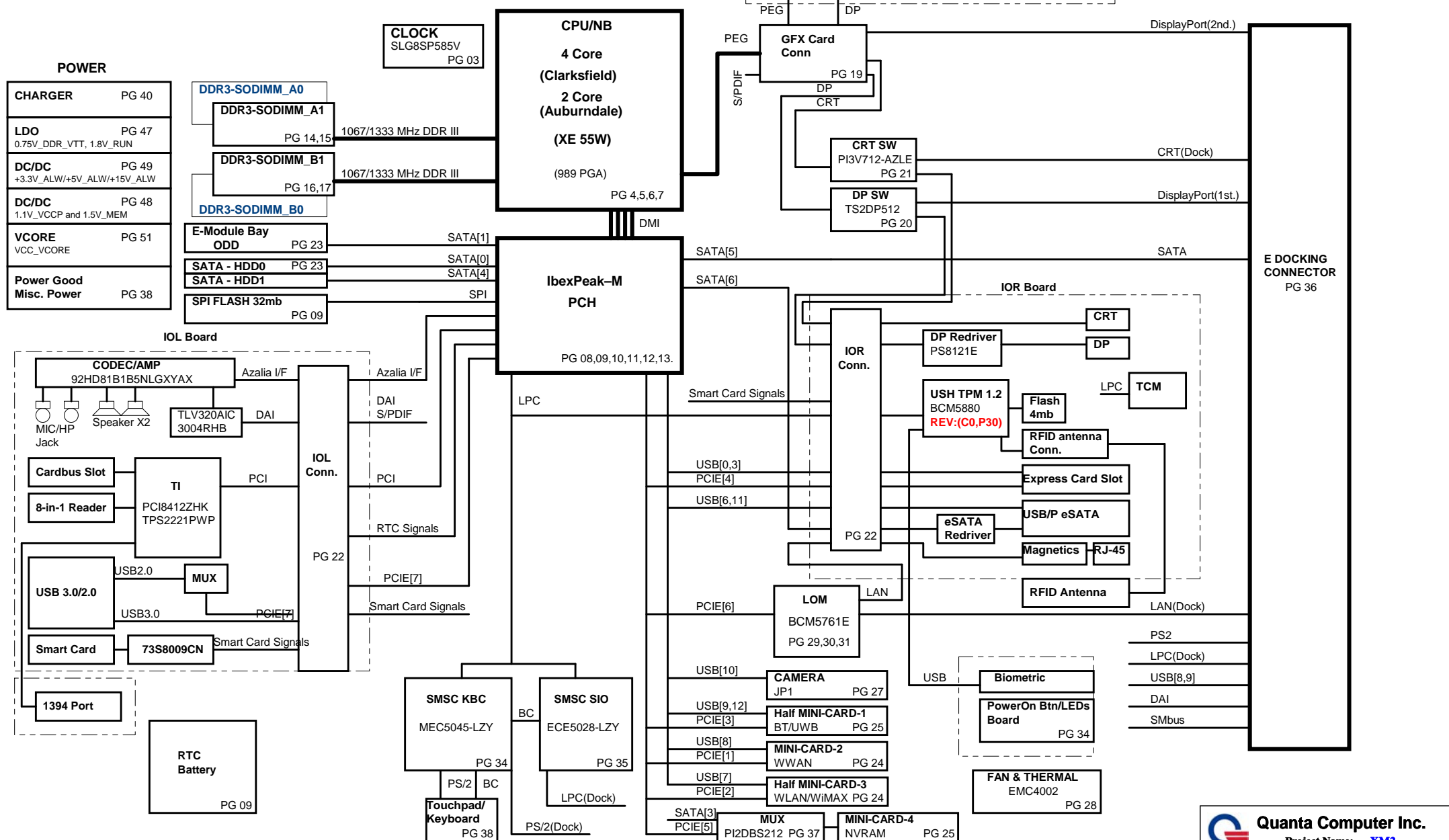
BOARD REV : D

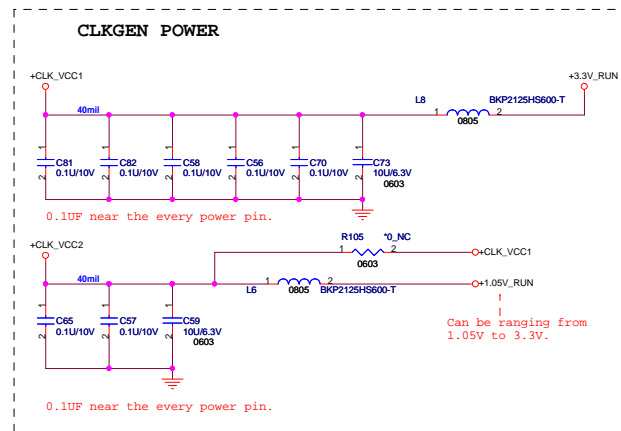
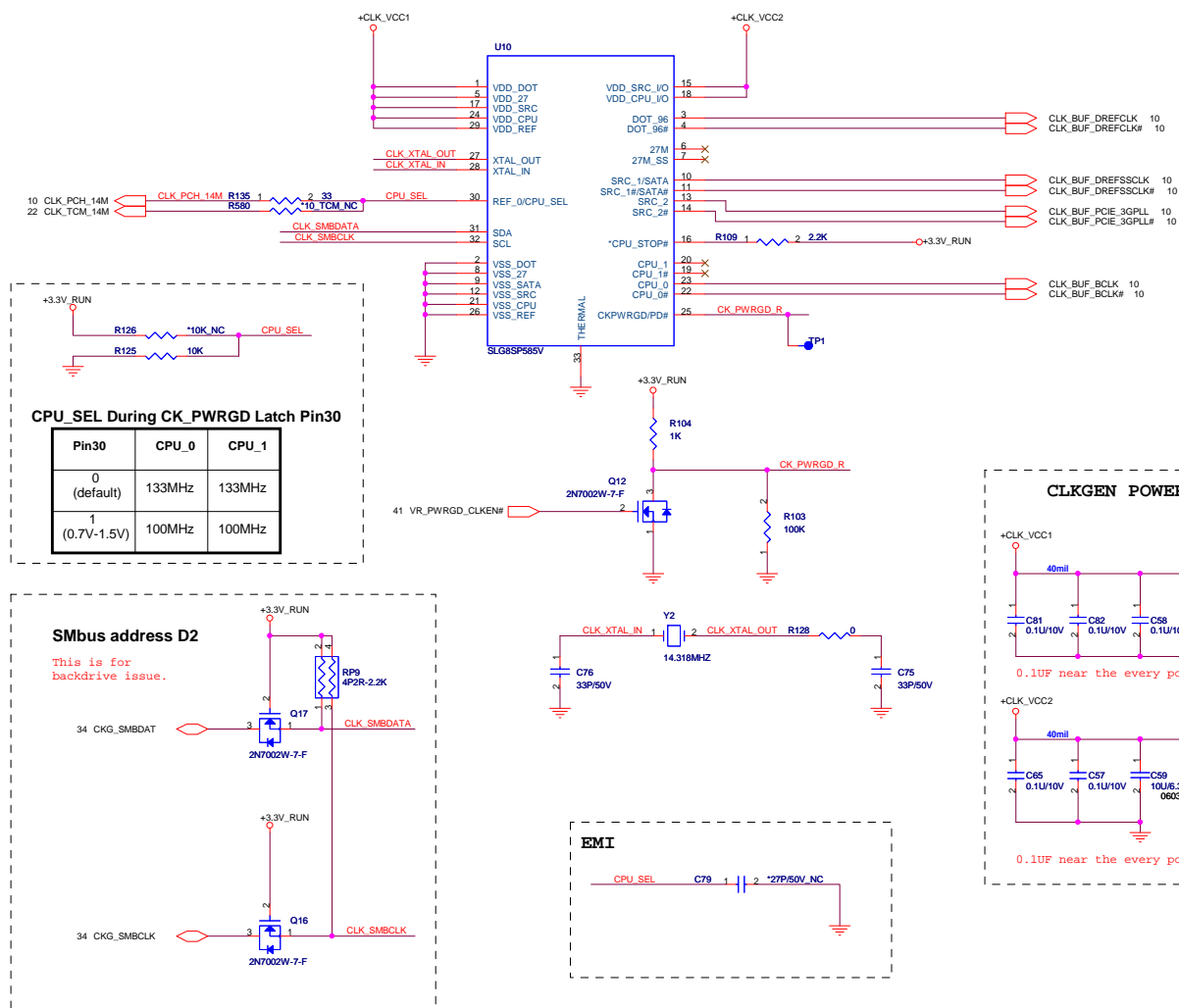
2009-07-24

 Quanta Computer Inc.		
Project Name: XM2		
Title: CoverPage		
Size:	Document Number: XM2_MB	Rev: B
Date: Friday, July 24, 2009 Sheet 1 of 55		

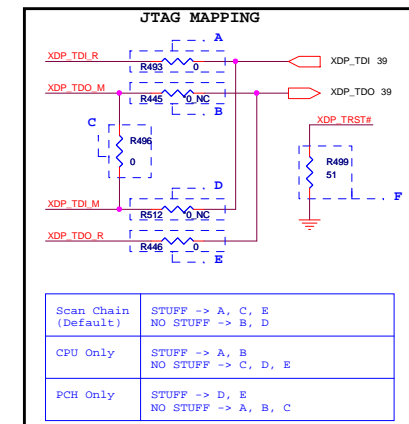
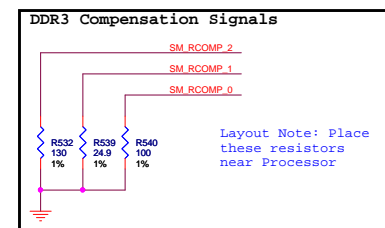
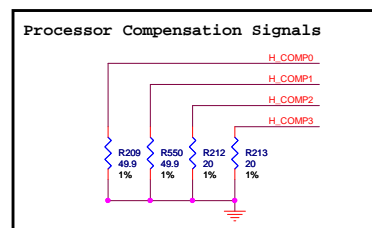
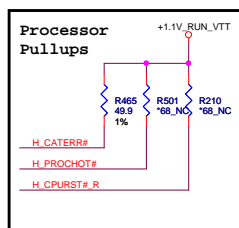
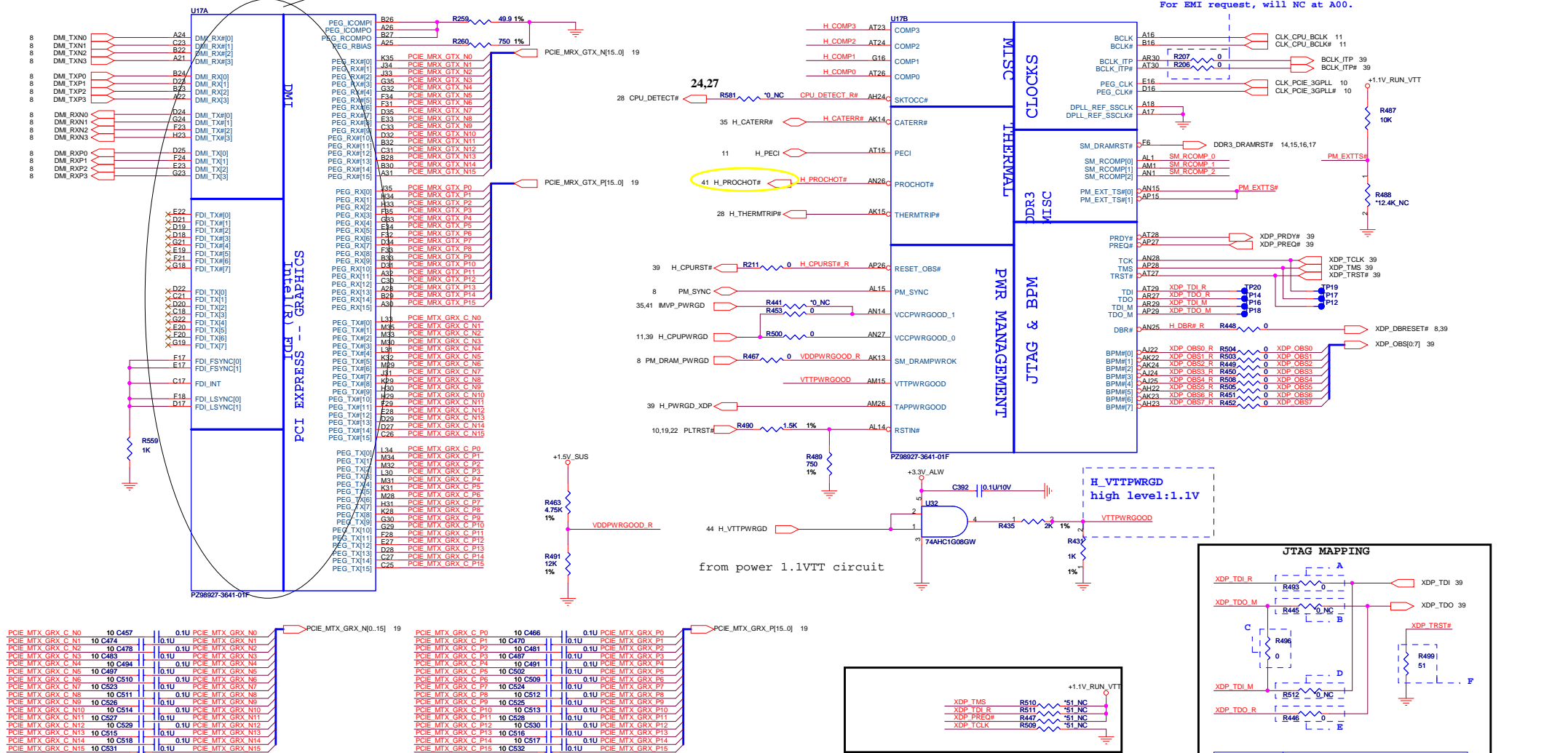


System Block Diagram of Reebok

PWA XXX, PWB XXX,
SCHEM XXX.
Board Ver : D
Date:20090716



1030CT: change CPU socket footprint from
mpga989_mcp_skt_37-5mm_sq TO rpga989-47989-socket



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

U17C

SA_DQ[0] A10
SA_DQ[1] C10
SA_DQ[2] C7
SA_DQ[3] A7
SA_DQ[4] B10
SA_DQ[5] D10
SA_DQ[6] E10
SA_DQ[7] A8
SA_DQ[8] D8
SA_DQ[9] E10
SA_DQ[10] E8
SA_DQ[11] E7
SA_DQ[12] E9
SA_DQ[13] B7
SA_DQ[14] E7
SA_DQ[15] C6
SA_DQ[16] H10
SA_DQ[17] S8
SA_DQ[18] K7
SA_DQ[19] J8
SA_DQ[20] G7
SA_DQ[21] G10
SA_DQ[22] J7
SA_DQ[23] J7
SA_DM[0] L7
SA_DM[1] L7
SA_DM[2] L7
SA_DM[3] M6
SA_DM[4] M6
SA_DM[5] L9
SA_DM[6] L6
SA_DM[7] K8
SA_DM[8] N8
SA_DM[9] P9
SA_DM[10] A9
SA_DM[11] A9
SA_DM[12] A9
SA_DM[13] A9
SA_DM[14] A9
SA_DM[15] A9
SA_DM[16] A9
SA_DM[17] A9
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SA_DM[58] A9
SA_DM[59] A9
SA_DM[60] A9
SA_DM[61] A9
SA_DM[62] A9
SA_DM[63] A9

DDR SYSTEM MEMORY - A

SA_BS[0] A3
SA_BS[1] A2
SA_BS[2] U7

SA_CAS# AE1C
SA_RAS# AB2C
SA_WE# AE3C

P298927-3641-01F

U17D

SB_DQ[0] B5
SB_DQ[1] A5
SB_DQ[2] C3
SB_DQ[3] B3
SB_DQ[4] E4
SB_DQ[5] A6
SB_DQ[6] A4
SB_DQ[7] C4
SB_DQ[8] D1
SB_DQ[9] D2
SB_DQ[10] E1
SB_DQ[11] F1
SB_DQ[12] C2
SB_DQ[13] E5
SB_DQ[14] E3
SB_DQ[15] G4
SB_DQ[16] G5
SB_DQ[17] J6
SB_DQ[18] J3
SB_DQ[19] G1
SB_DQ[20] G5
SB_DQ[21] J2
SB_DQ[22] J2
SB_DQ[23] J2
SB_DQ[24] J5
SB_DQ[25] L3
SB_DQ[26] M1
SB_DQ[27] M1
SB_DQ[28] K4
SB_DQ[29] M4
SB_DQ[30] N5
SB_DQ[31] A3
SB_DQ[32] A3
SB_DQ[33] A3
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SB_DQ[63] A3

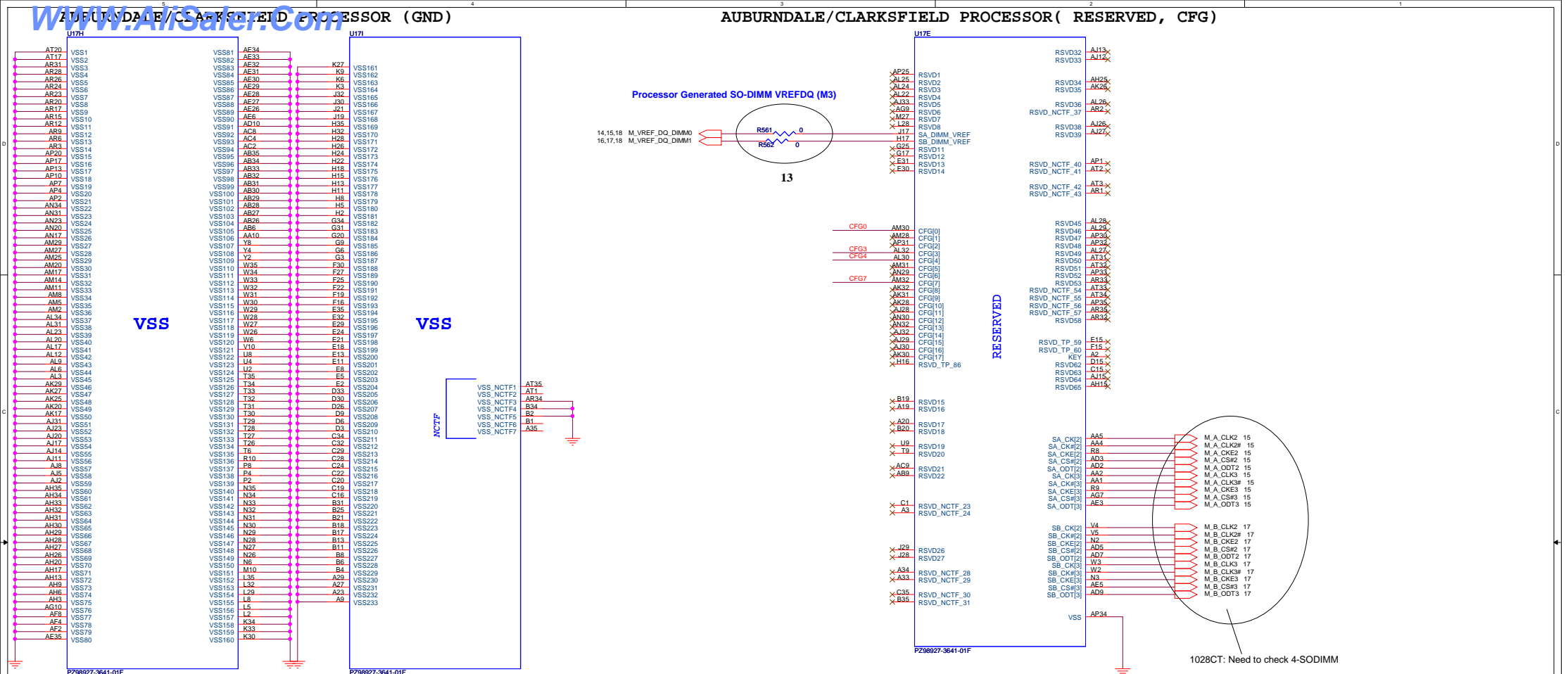
DDR SYSTEM MEMORY - B

SB_BS[0] A3
SB_BS[1] A2
SB_BS[2] U7

SB_CAS# AE1C
SB_RAS# AB2C
SB_WE# AE3C

P298927-3641-01F



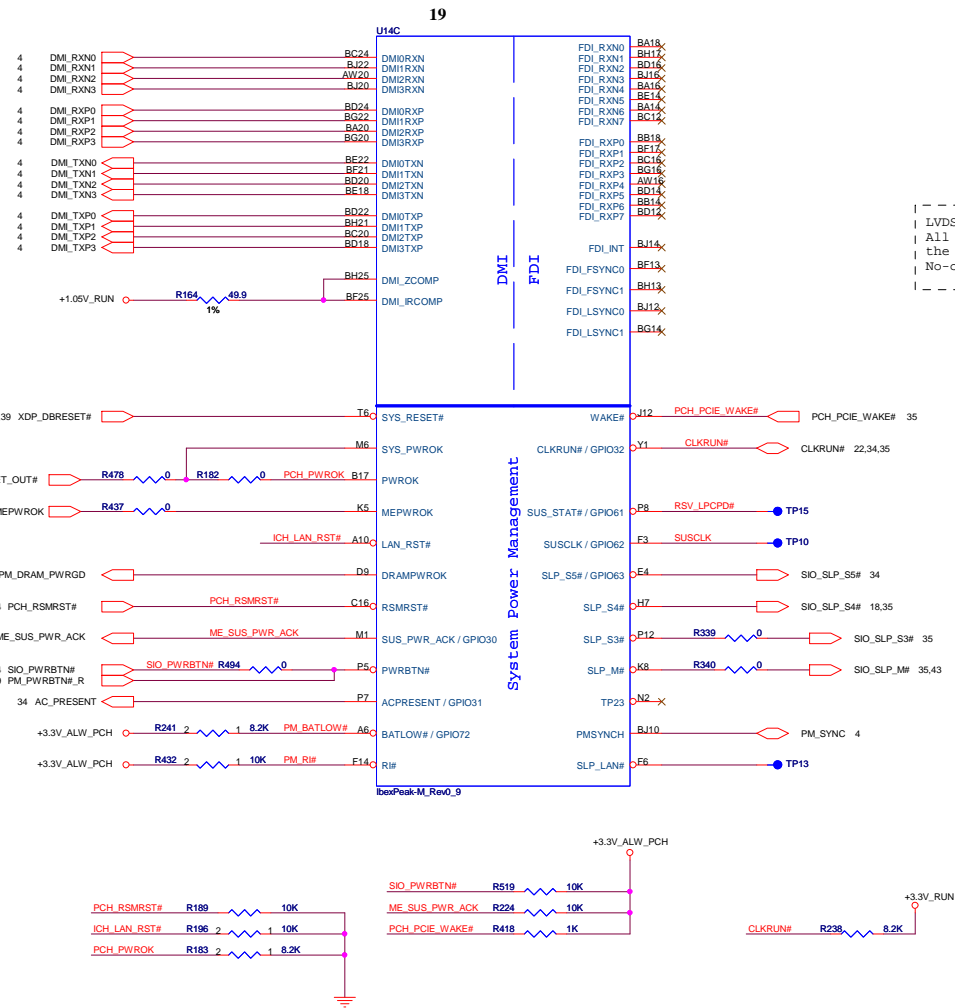


The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



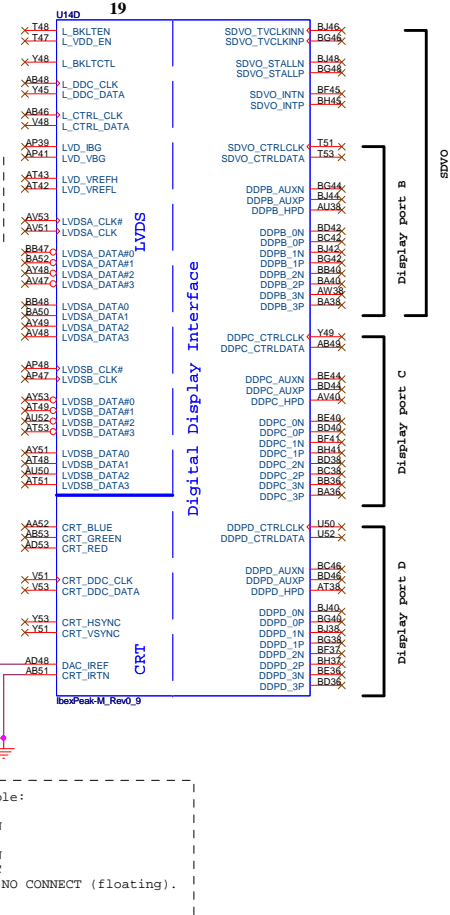
	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed
CFG7 (Clarkfield (only for early samples pre-ES1))	Common motherboard design	For early samples pre-ES1 CFD

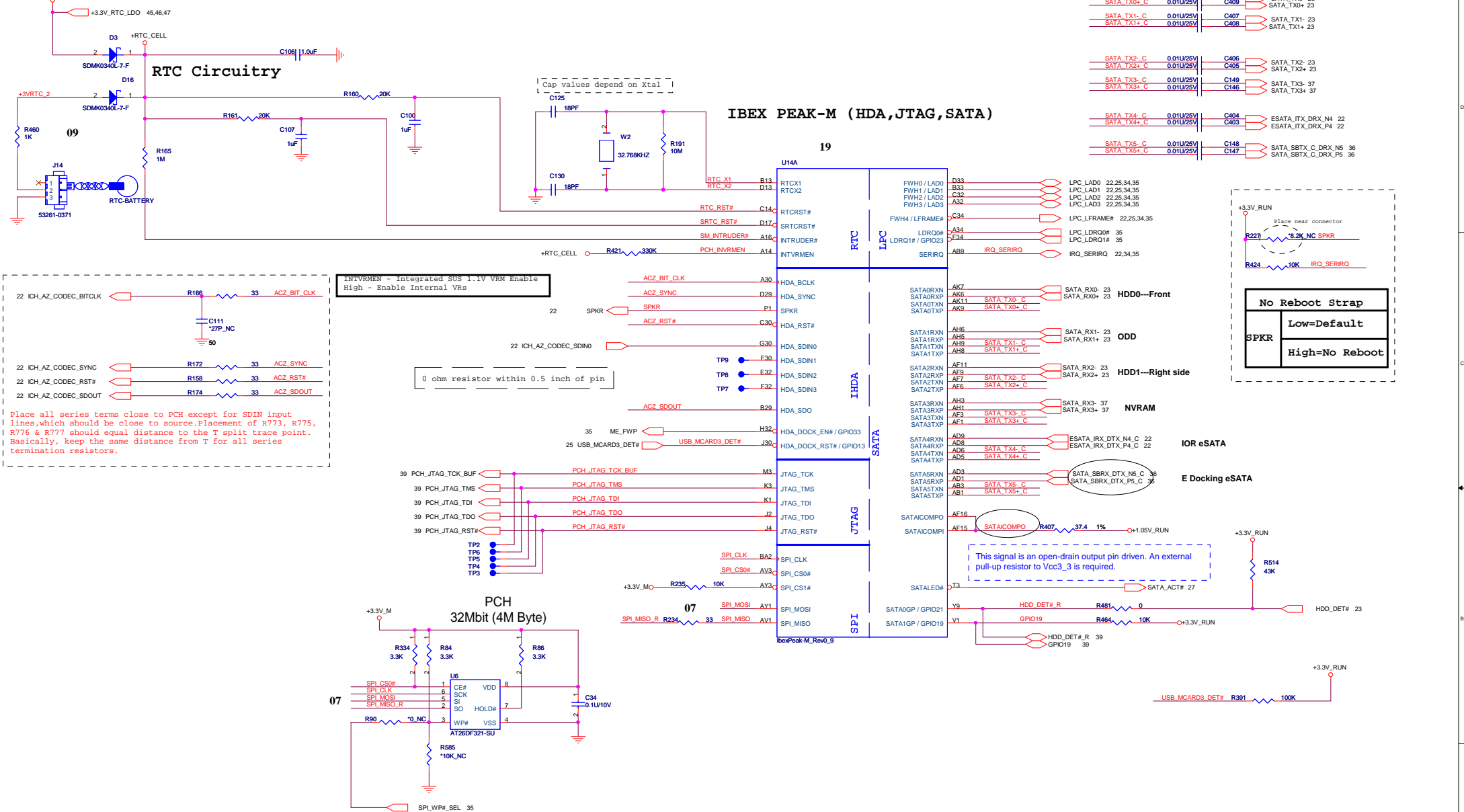
IBEX PEAK-M (DMI, FDI, GPIO)

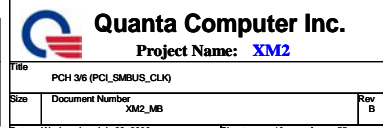


LVDS Disable:
All signals associated with the interface can be left as No-connects.

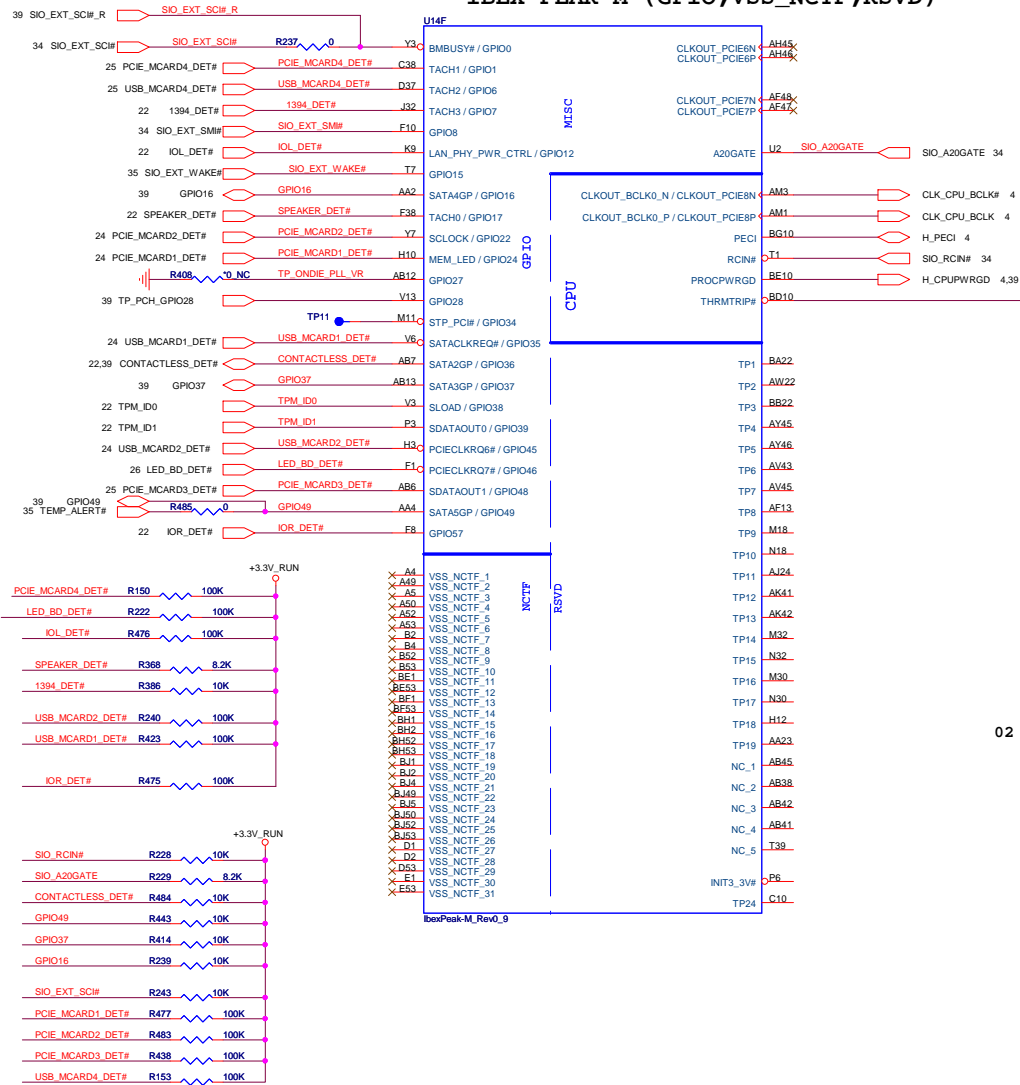
IBEX PEAK-M (LVDS, DDI)



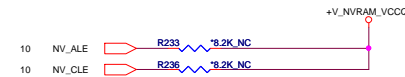




IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



02



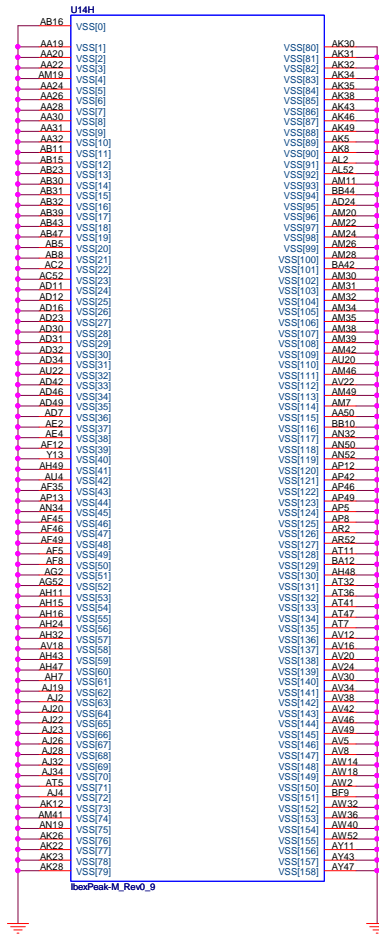
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

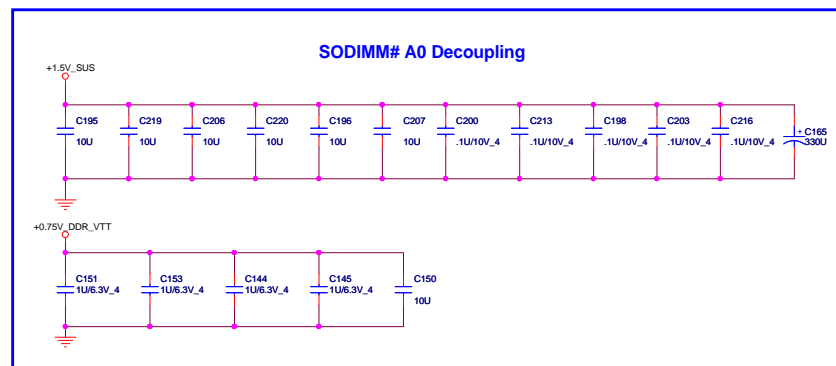
Danbury Technology Enabled	
NV_ALE	High = Enable(Default) Low = Disable



IBEX PEAK-M (GND)

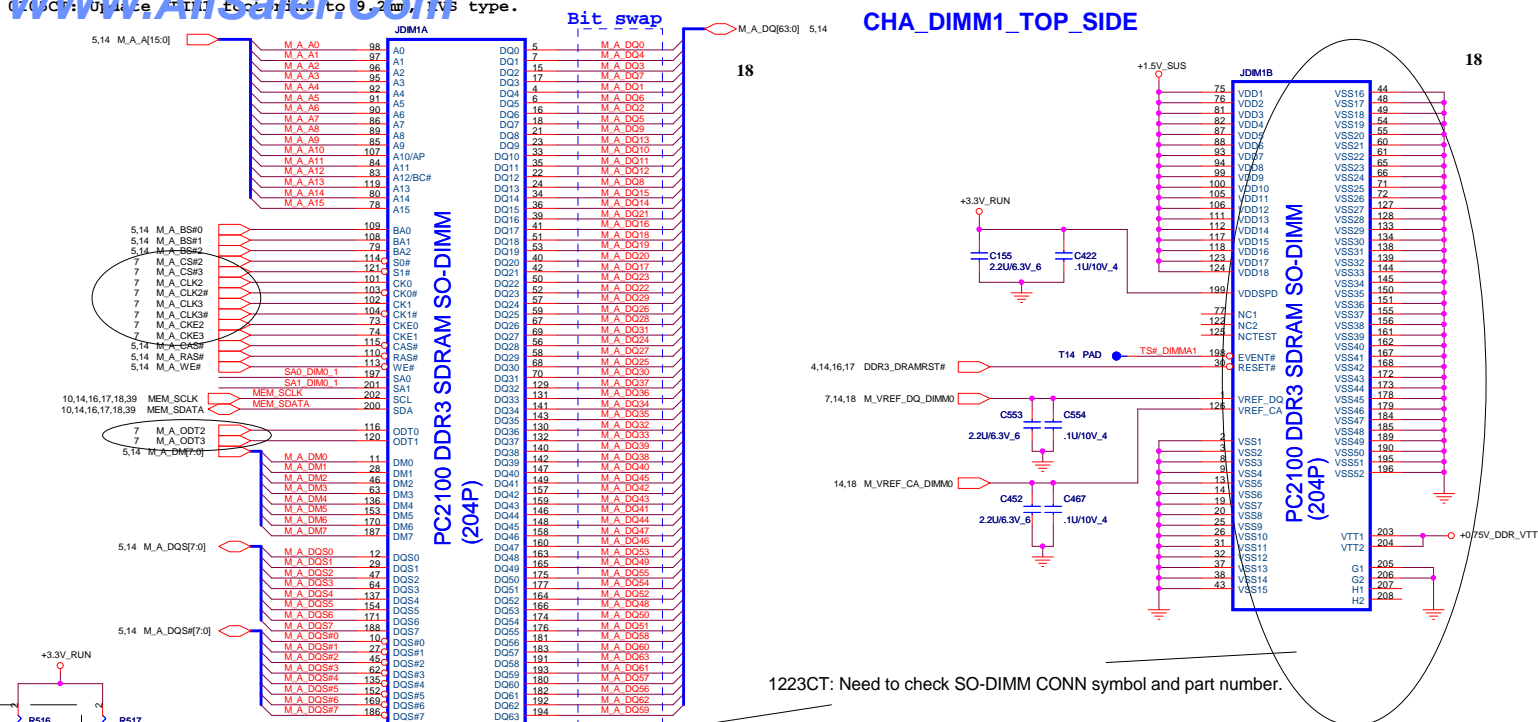
19





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

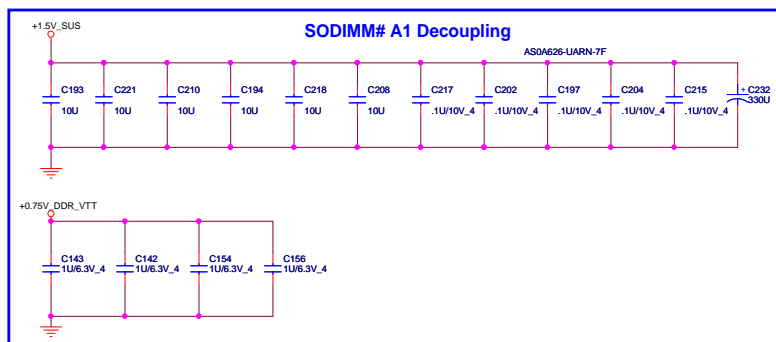
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

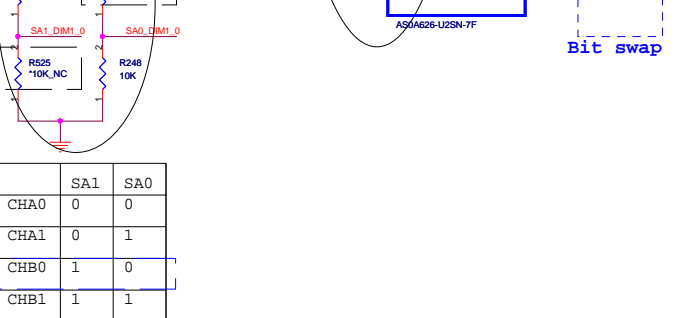
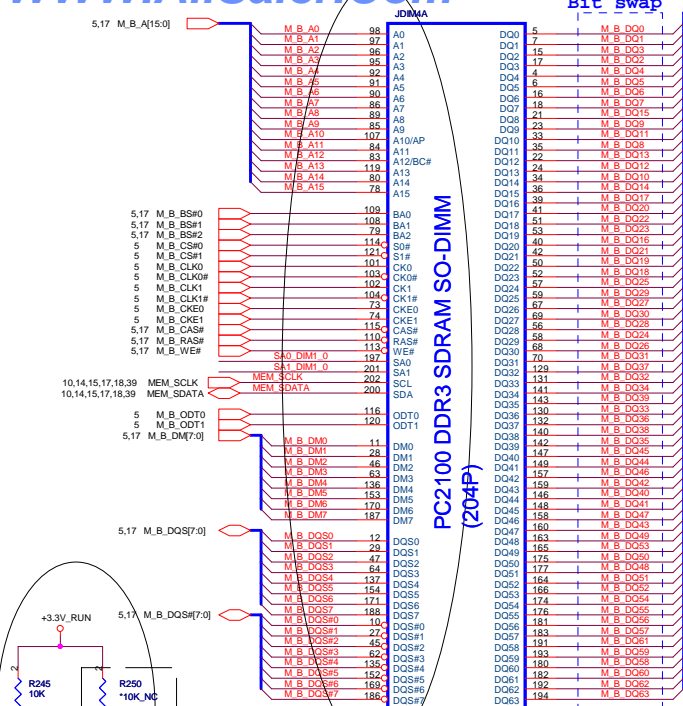


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0xA32

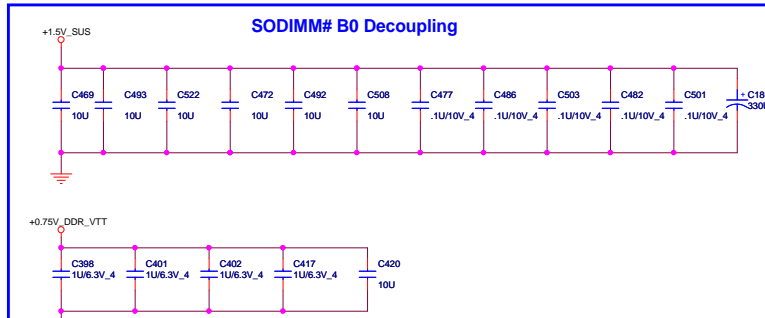
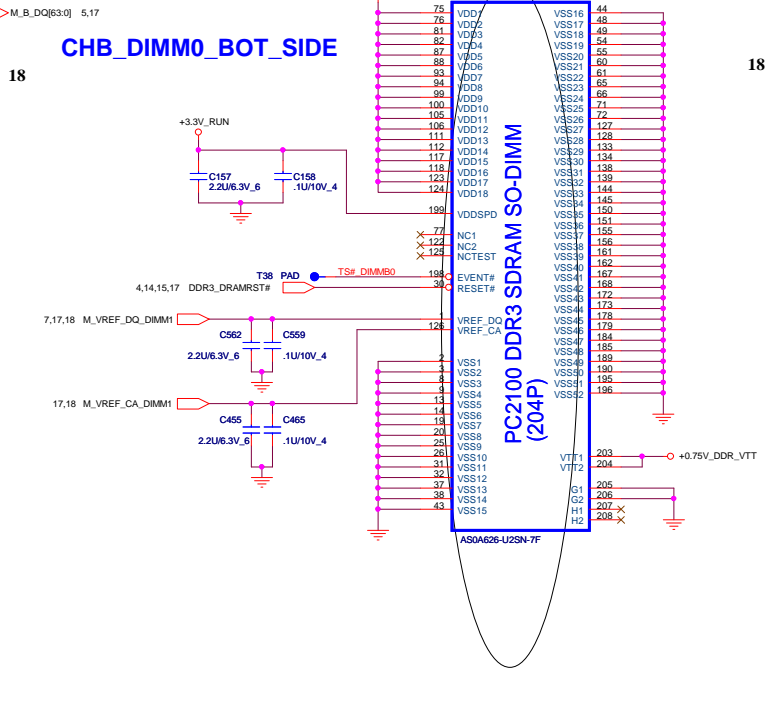
1223CT: Need to check SO-DIMM CONN symbol and part number.





	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



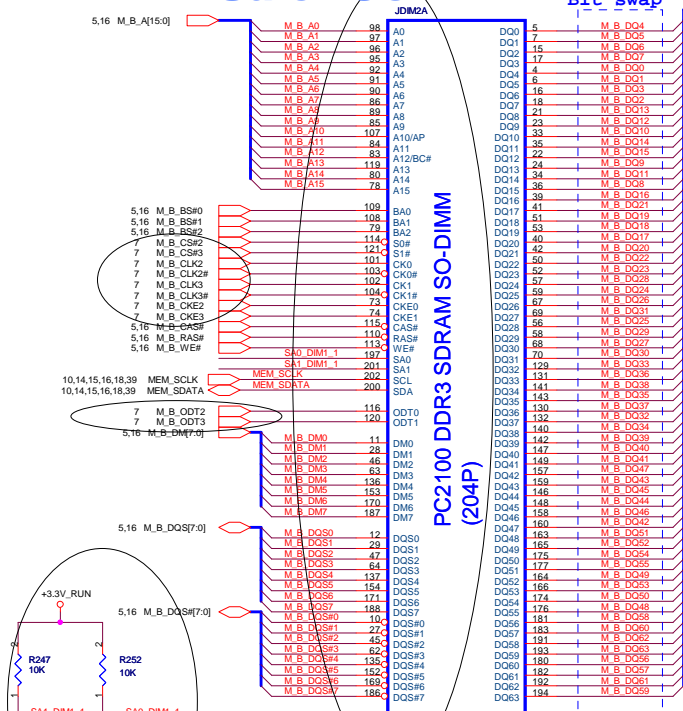
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

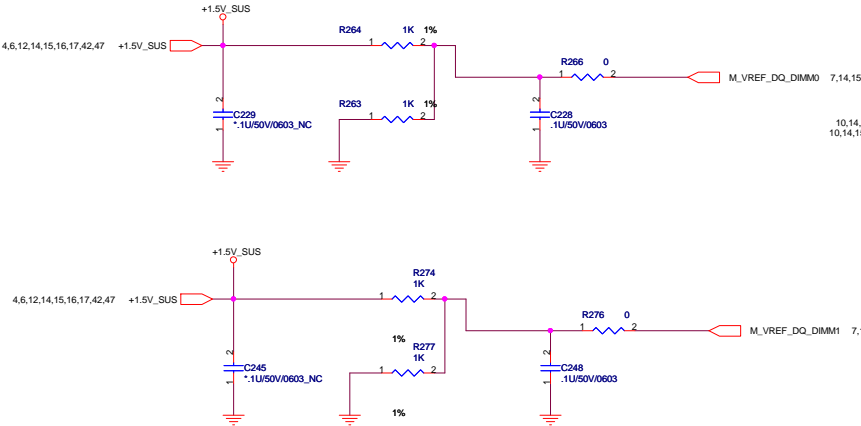


	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

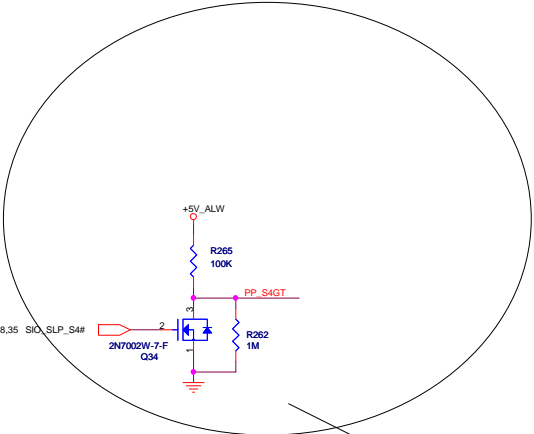
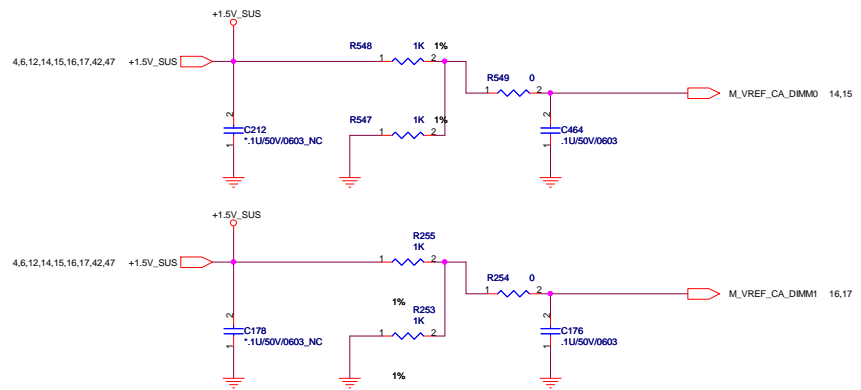
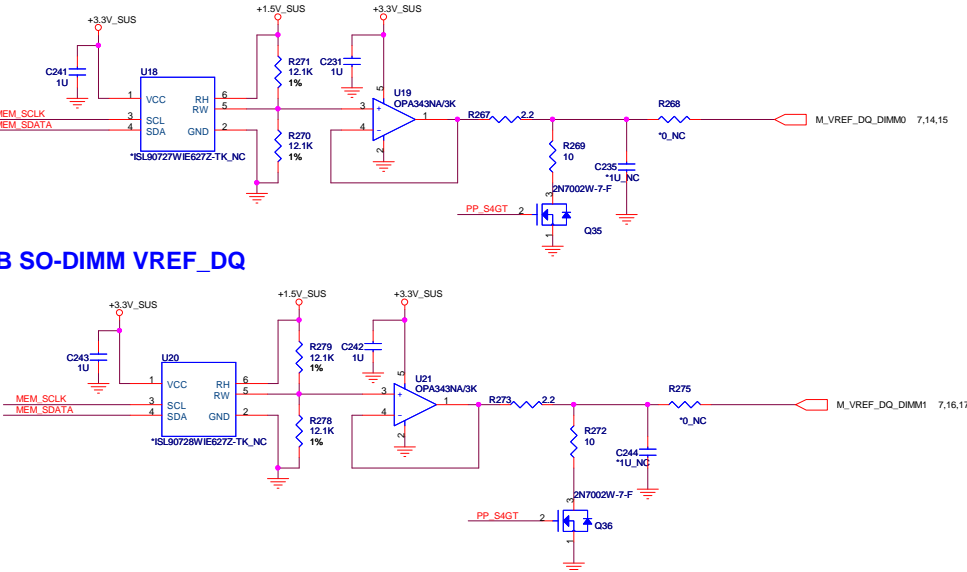
Note:
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34



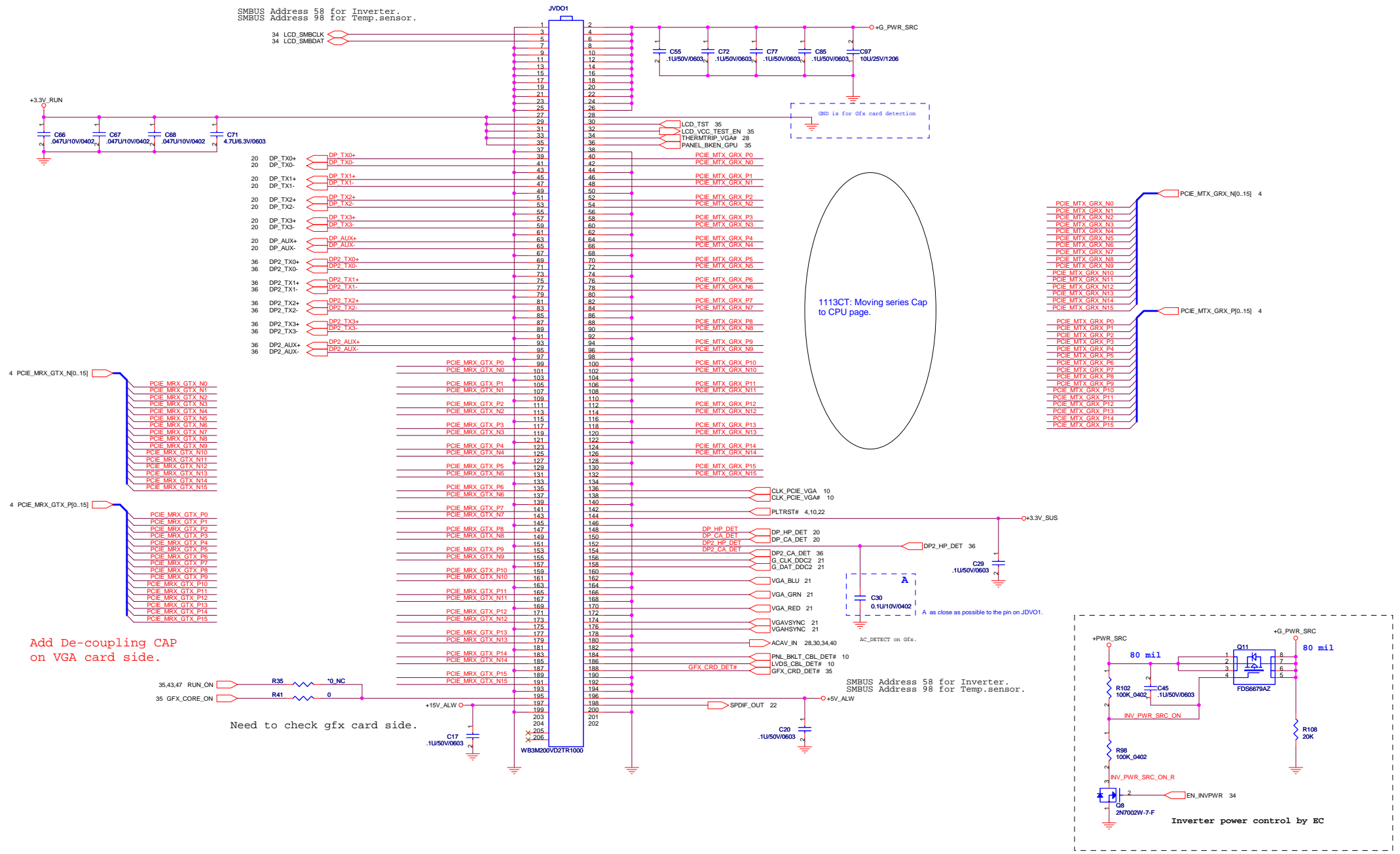
For CH A SO-DIMM VREF_DQ

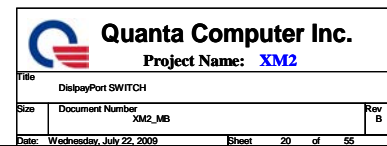


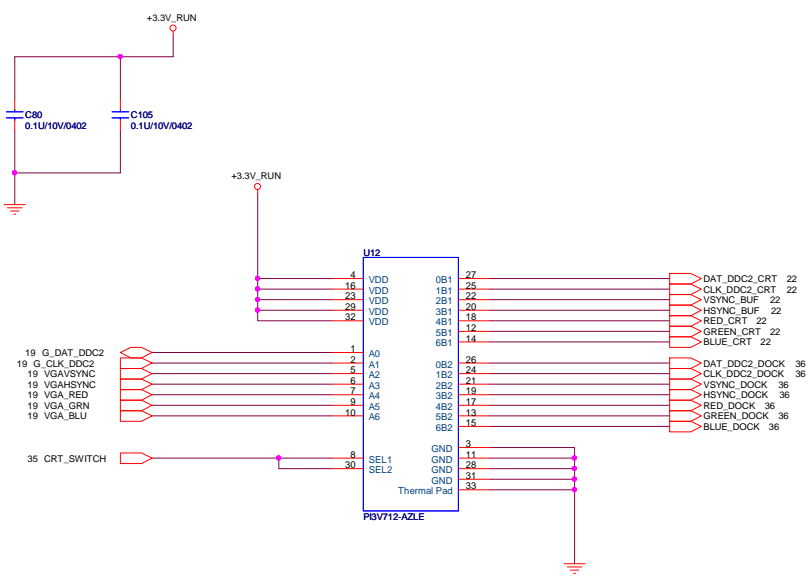
For CH B SO-DIMM VREF_DQ



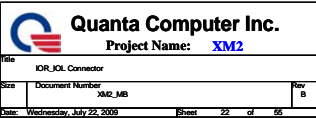
1203CT: Refer to FM6C







Input SELx	Input/Output An	Function	
L	nB1	An=nB1	nB2 hing impedance mode
H	nB2	An=nB2	nB1 hing impedance mode



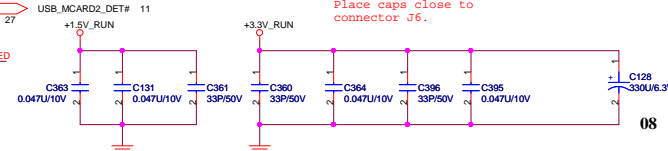
	D(3)	
(2)		S(1)

EN	DO	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

TI:SN75LVCP41
MAXIM:MAX4951

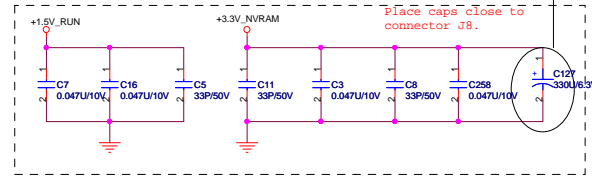
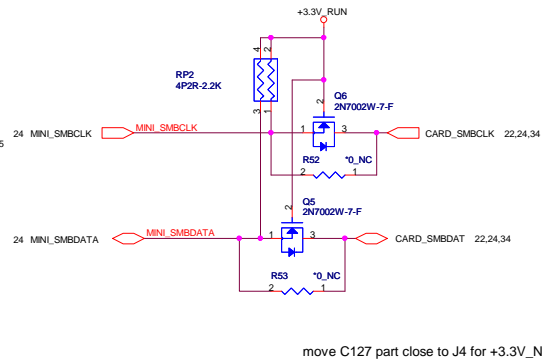
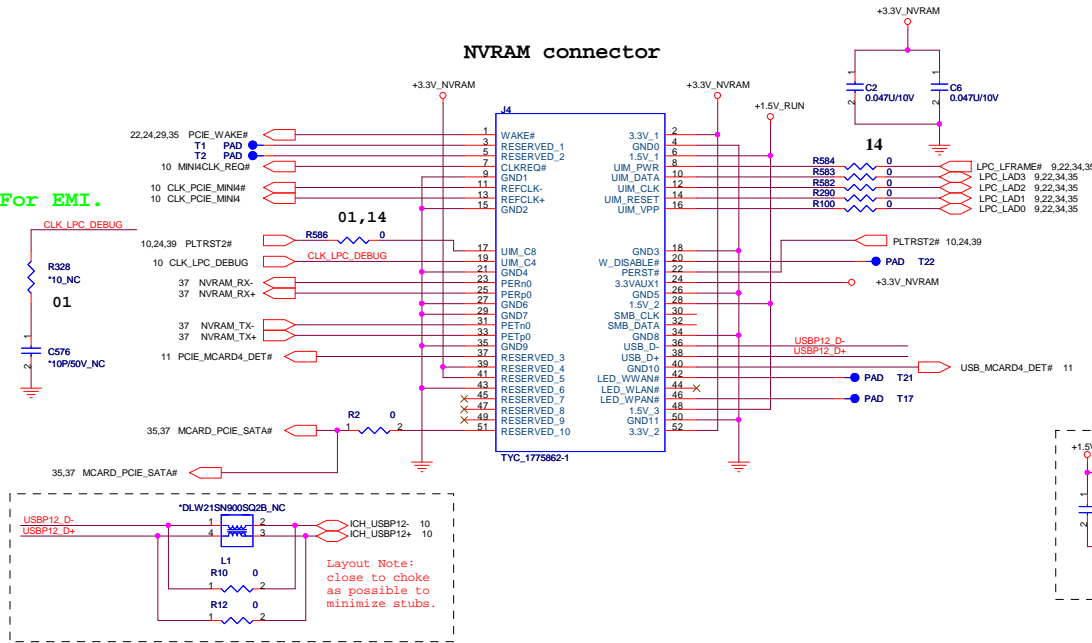
04,10

Sim card circuit moves to IOR.

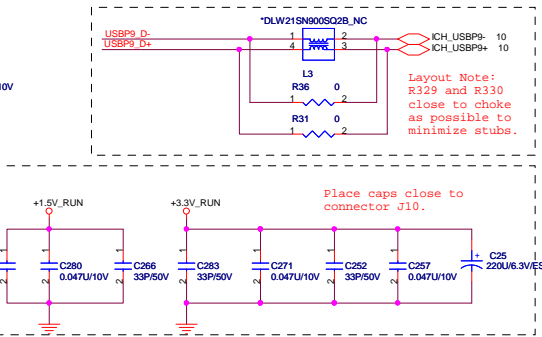
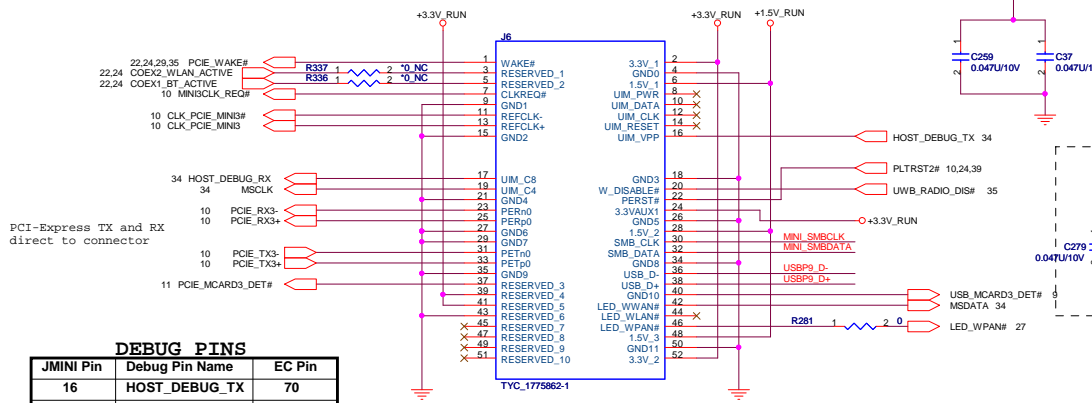


NVRAM connector

For EMI.



MiniCard UWB/BT connector



DEBUG PINS

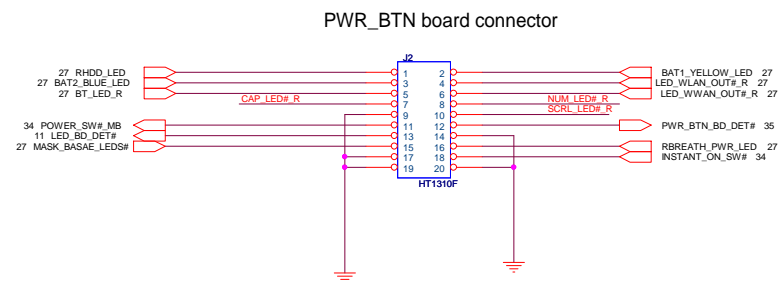
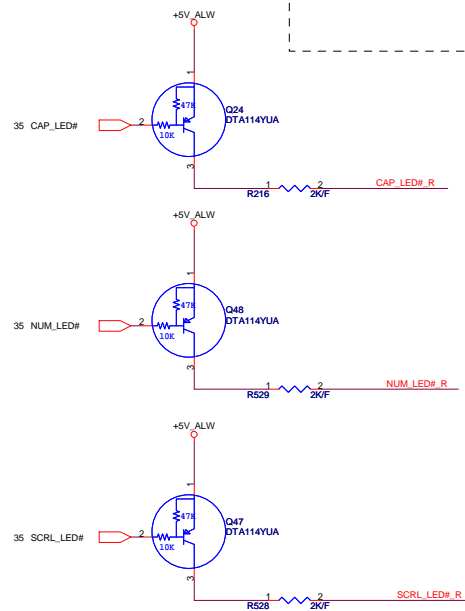
JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



Quanta Computer Inc.

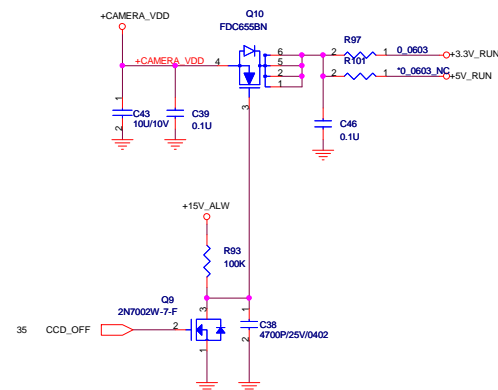
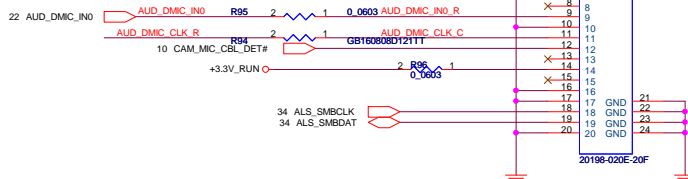
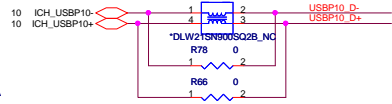
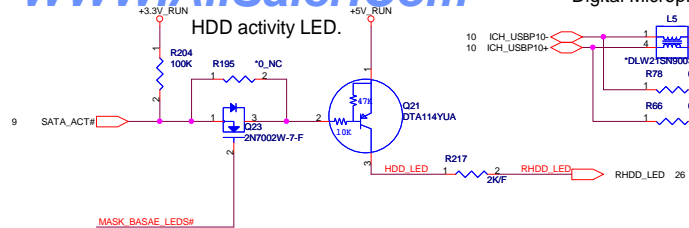
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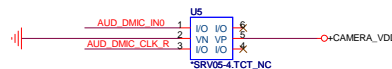
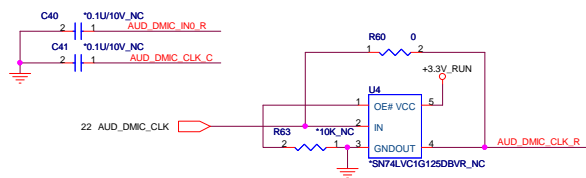
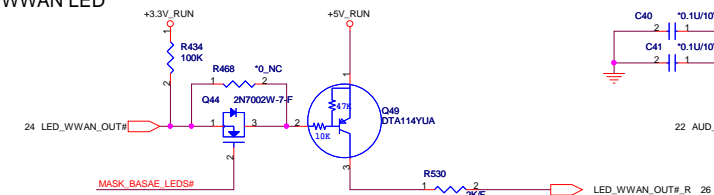


Digital Microphone & Camera

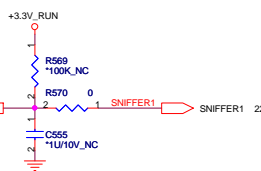
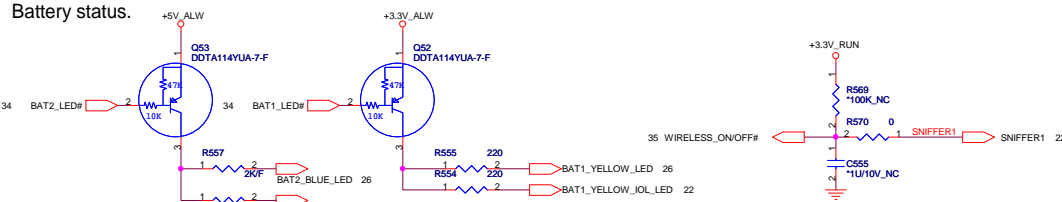
0219GC: Change to 15 pin connector per ME request,
Need to make new CCD cable for Reebok.



WWAN LED

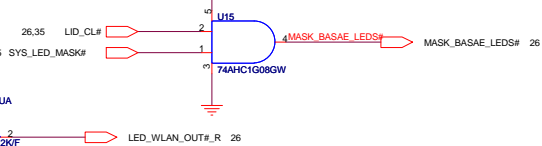
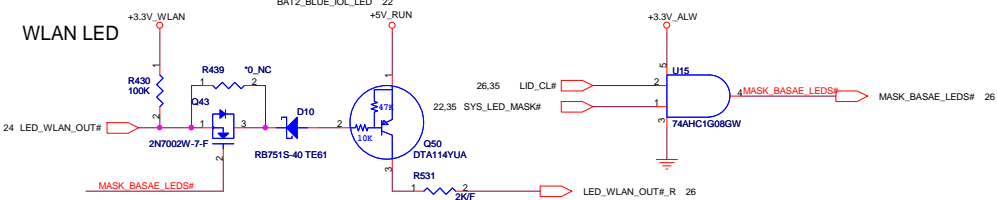


Battery status.

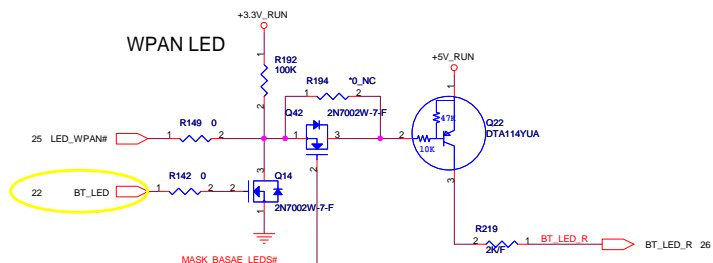


	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base LEDs (Lid Closed)	1	0
Do Not Mask LEDs (Lid Open)	1	1

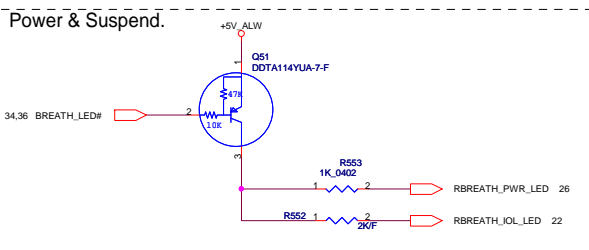
WLAN LED

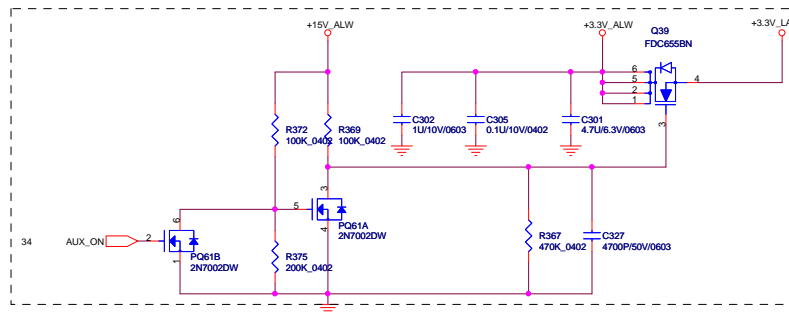
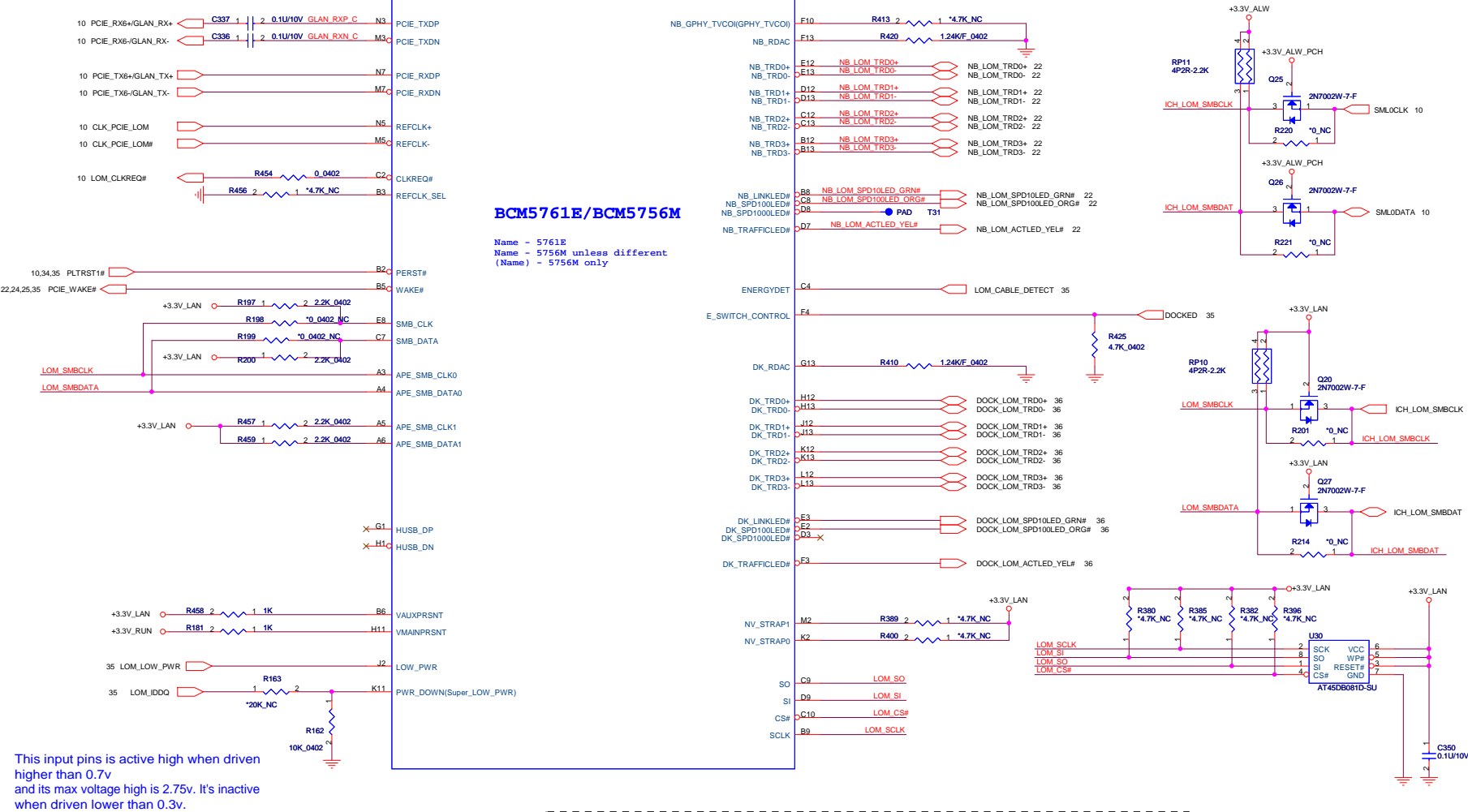


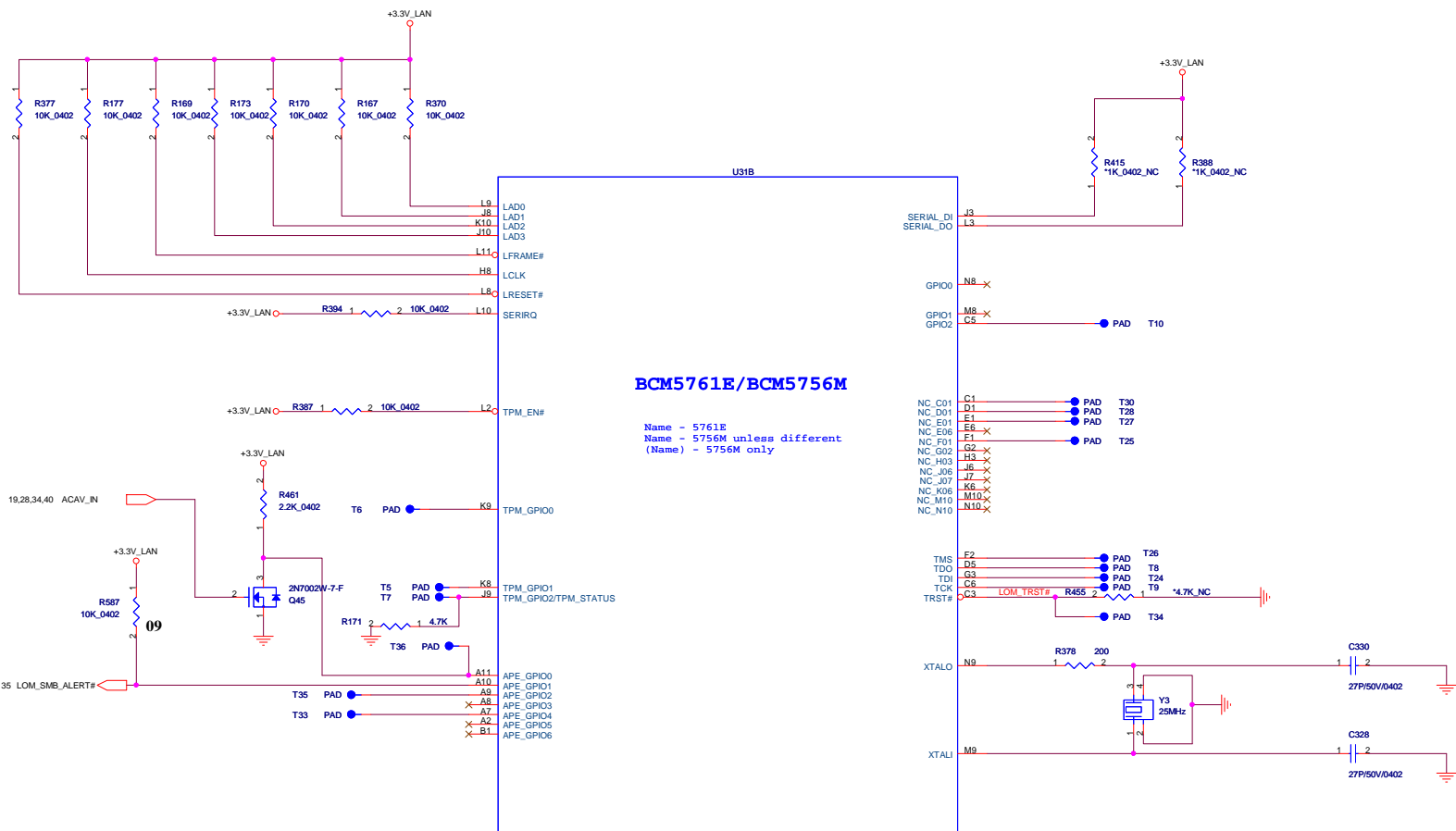
WPAN LED

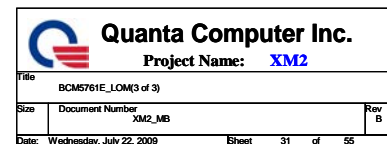



Power & Suspend.










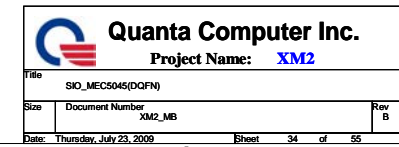
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Title TPM For China			
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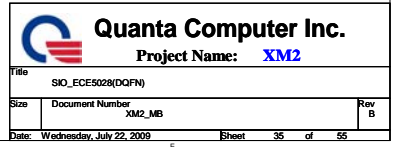
ECE 1099 was deleted

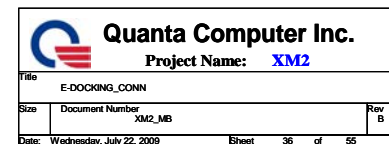
Bluetooth

Little Stone moves to IOL.

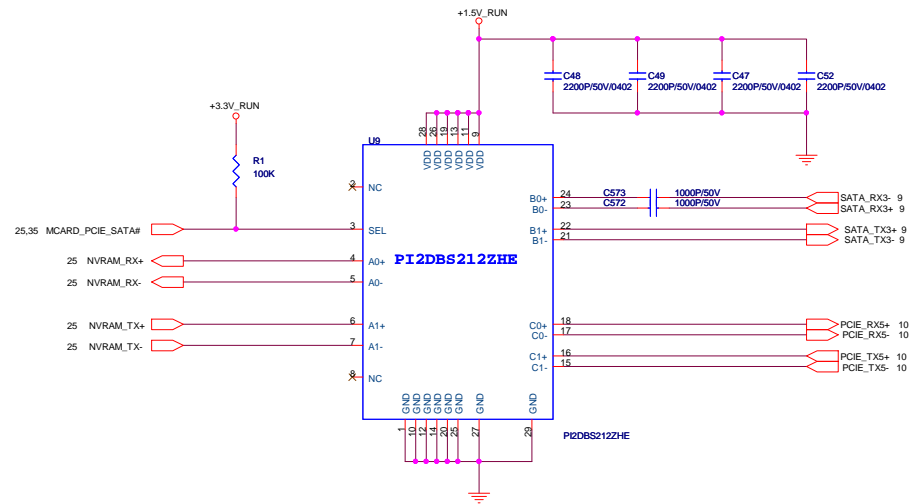
 Quanta Computer Inc.		
Project Name: XM2		
Title: ECE1099 AND Bluetooth		
Size	Document Number: XM2_MB	Rev: B
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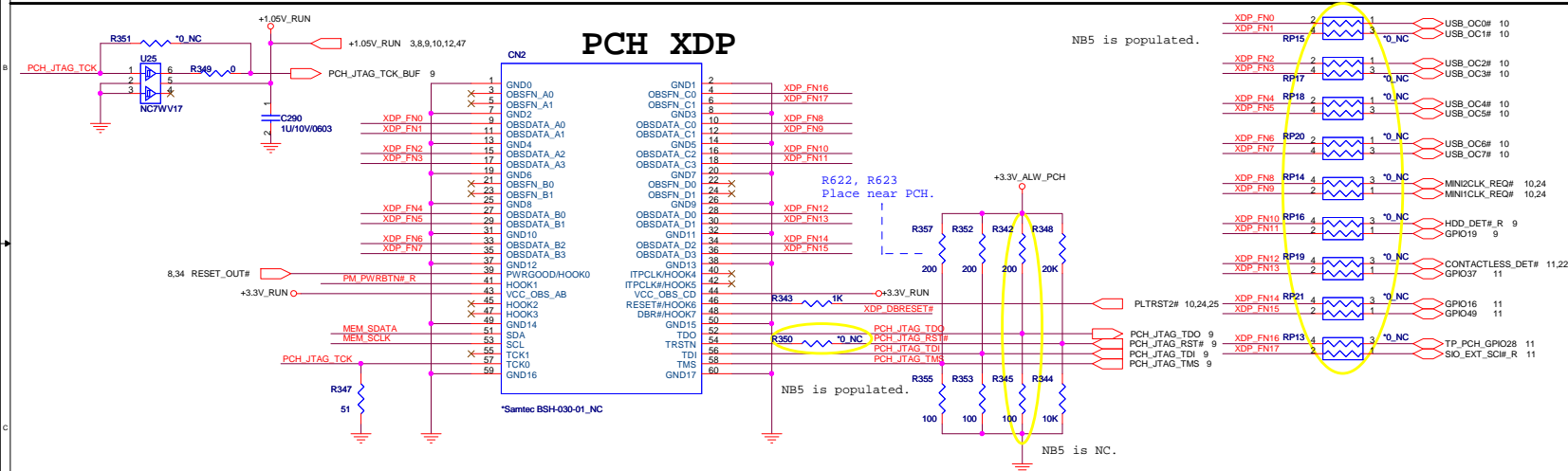
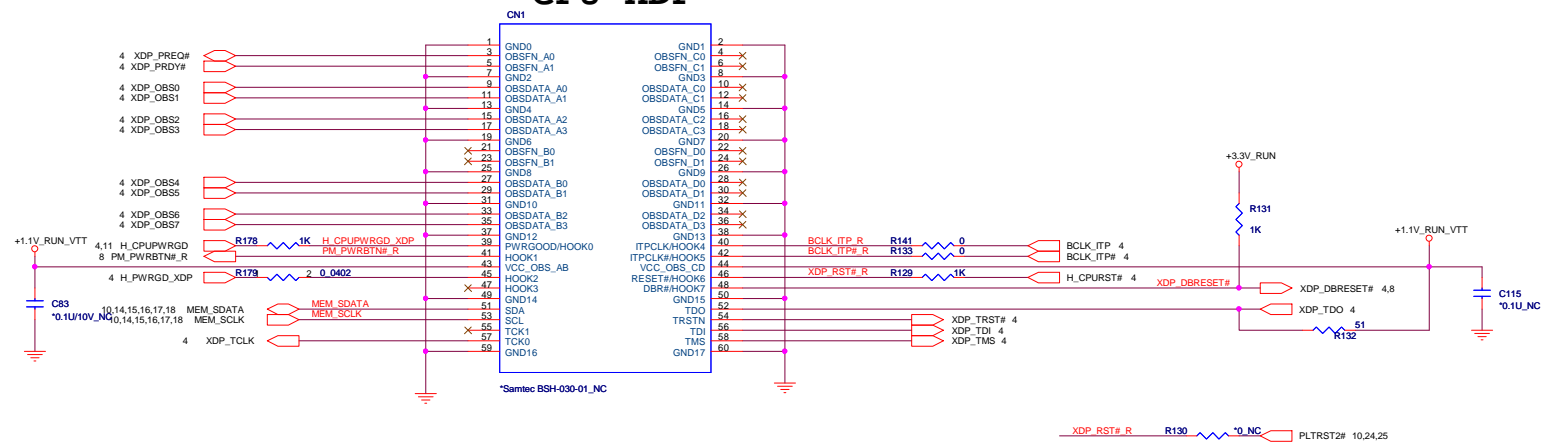
NVRAM MUX IC



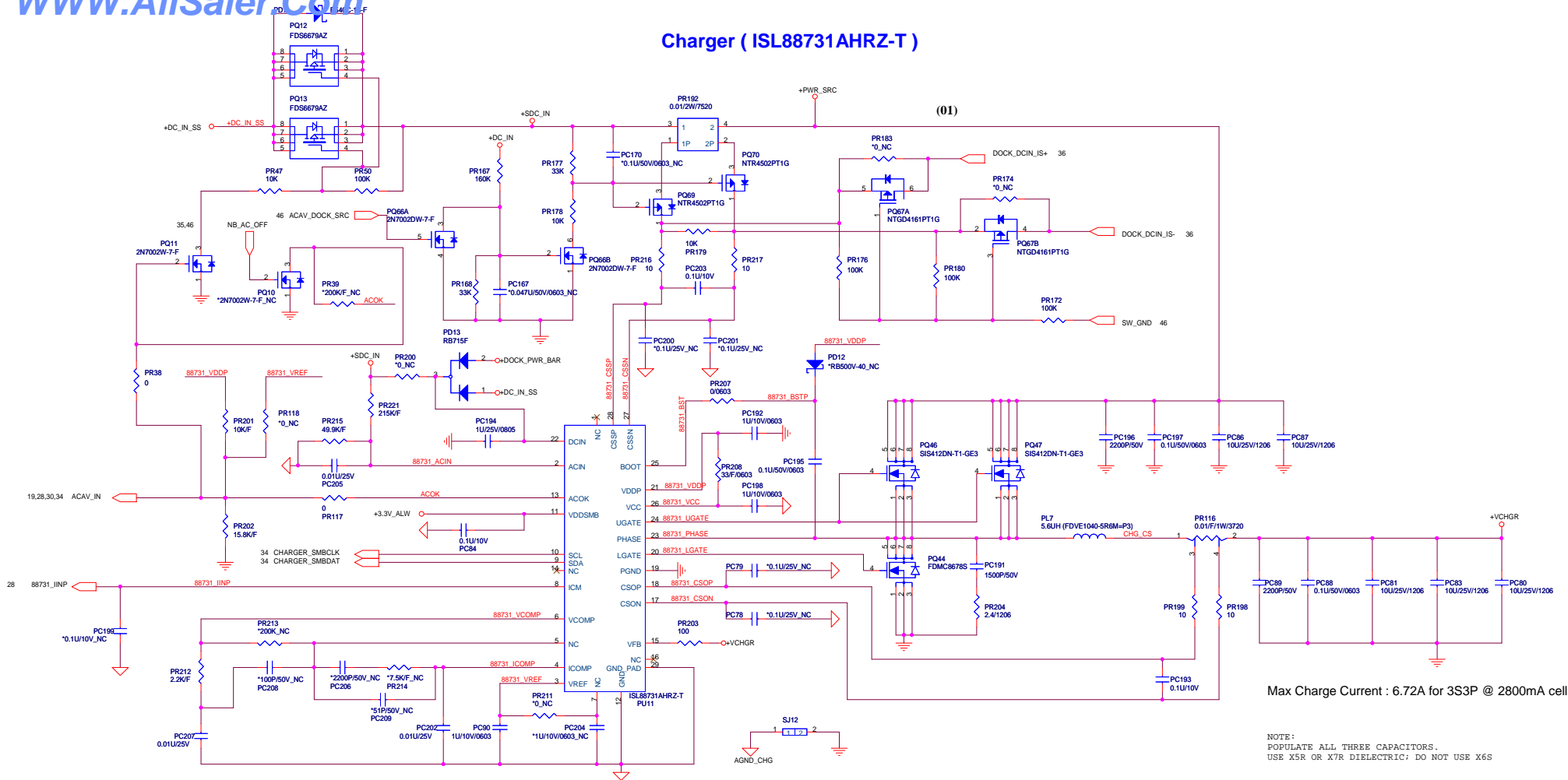
Function	SEL
Port A to Port B	L
Port A to Port C	H

		Quanta Computer Inc.	
		Project Name: XM2	
Title System Power Good(Blank)			
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CPU XDP

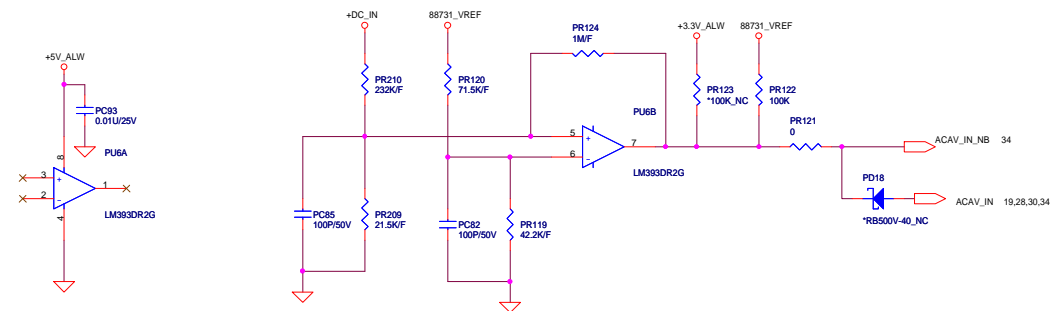


Charger (ISL88731AHRZ-T)



Max Charge Current : 6.72A for 3S3P @ 2800mA cell

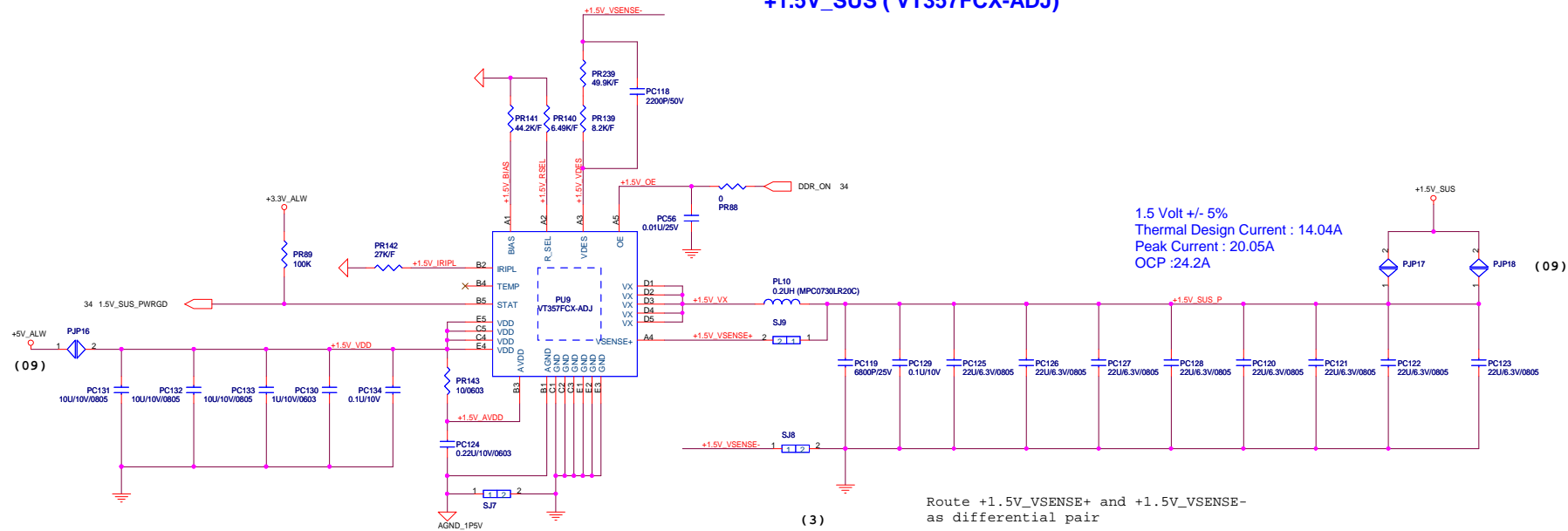
NOTE:
POPULATE ALL THREE CAPACITORS.
USE X5R OR X7R DIELECTRIC; DO NOT USE X6S





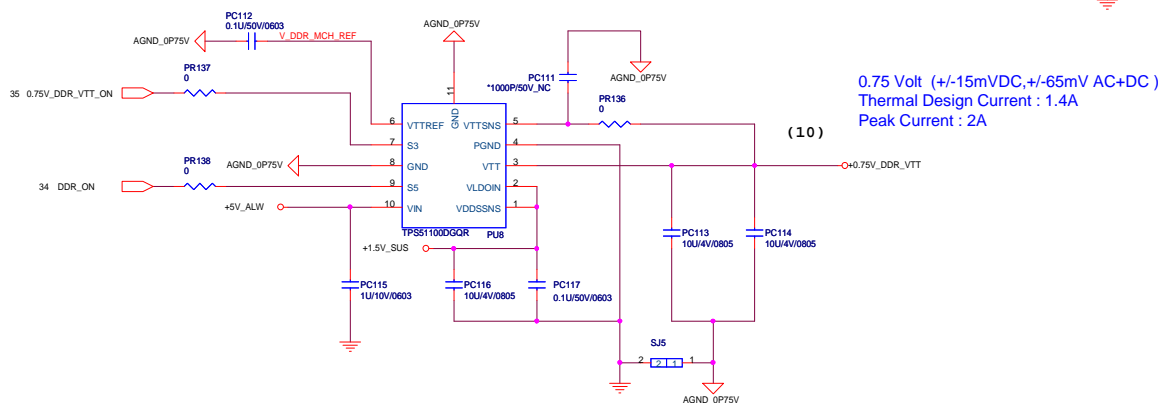
VCORE_LL_SELECT	Load Line
High	-1.9mOhm
Low	-1.6mOhm

+1.5V_SUS (VT357FCX-ADJ)

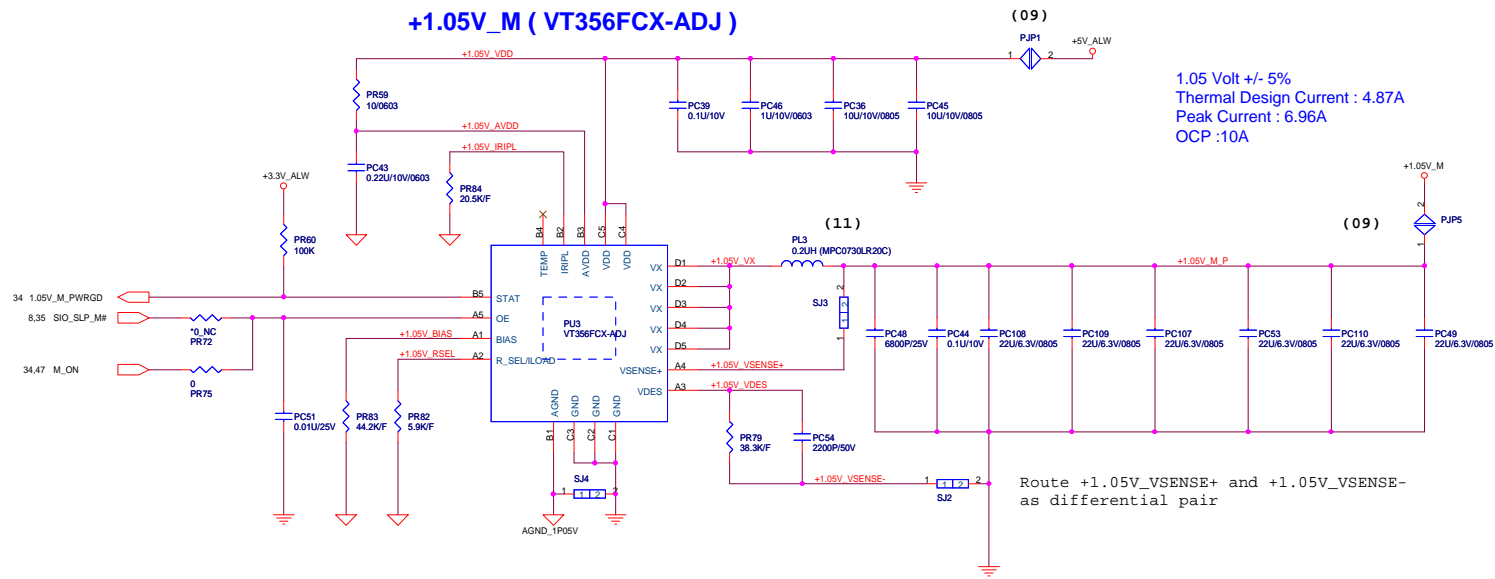


1.5V_SUS_CNTRL1	1.5V_SUS_CNTRL2	1.5V_SUS
Low	Low	1.65V
High	Low	1.6V
Low	High	1.55V
High	High	1.5V

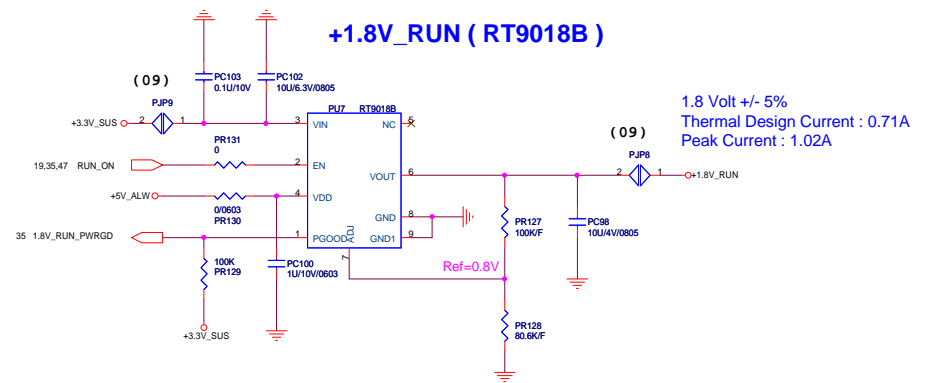
+0.75V_DDR_VTT (TPS51100DGQR)



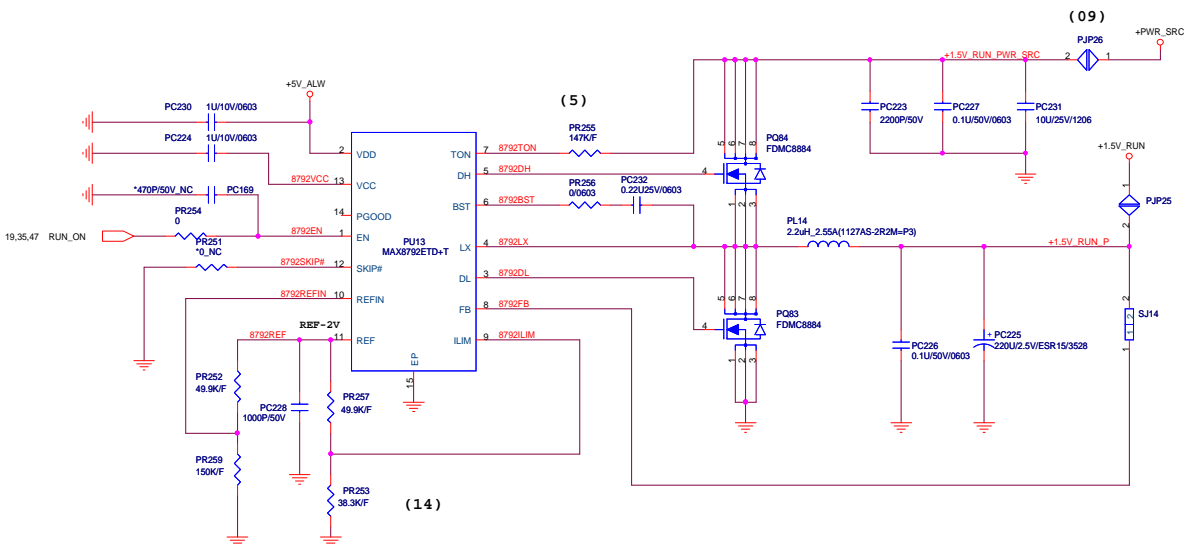
+1.05V_M (VT356FCX-ADJ)




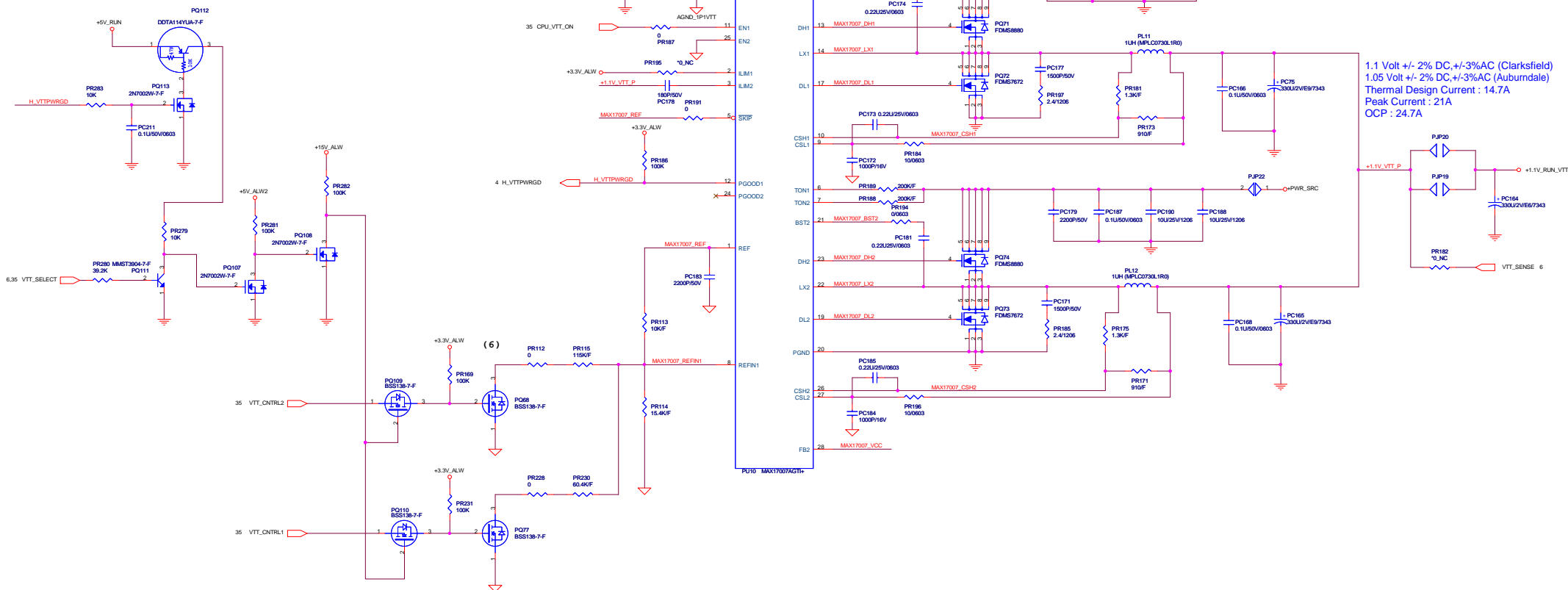
+1.8V_RUN (RT9018B)



1.5 Volt +/- 5%
Thermal Design Current : 1.52A
Peak Current : 2.18A
OCP :3.1A



 Quanta Computer Inc. Project Name: Reebok		NR
Title +1.V_VTT+1.05V_VTT		
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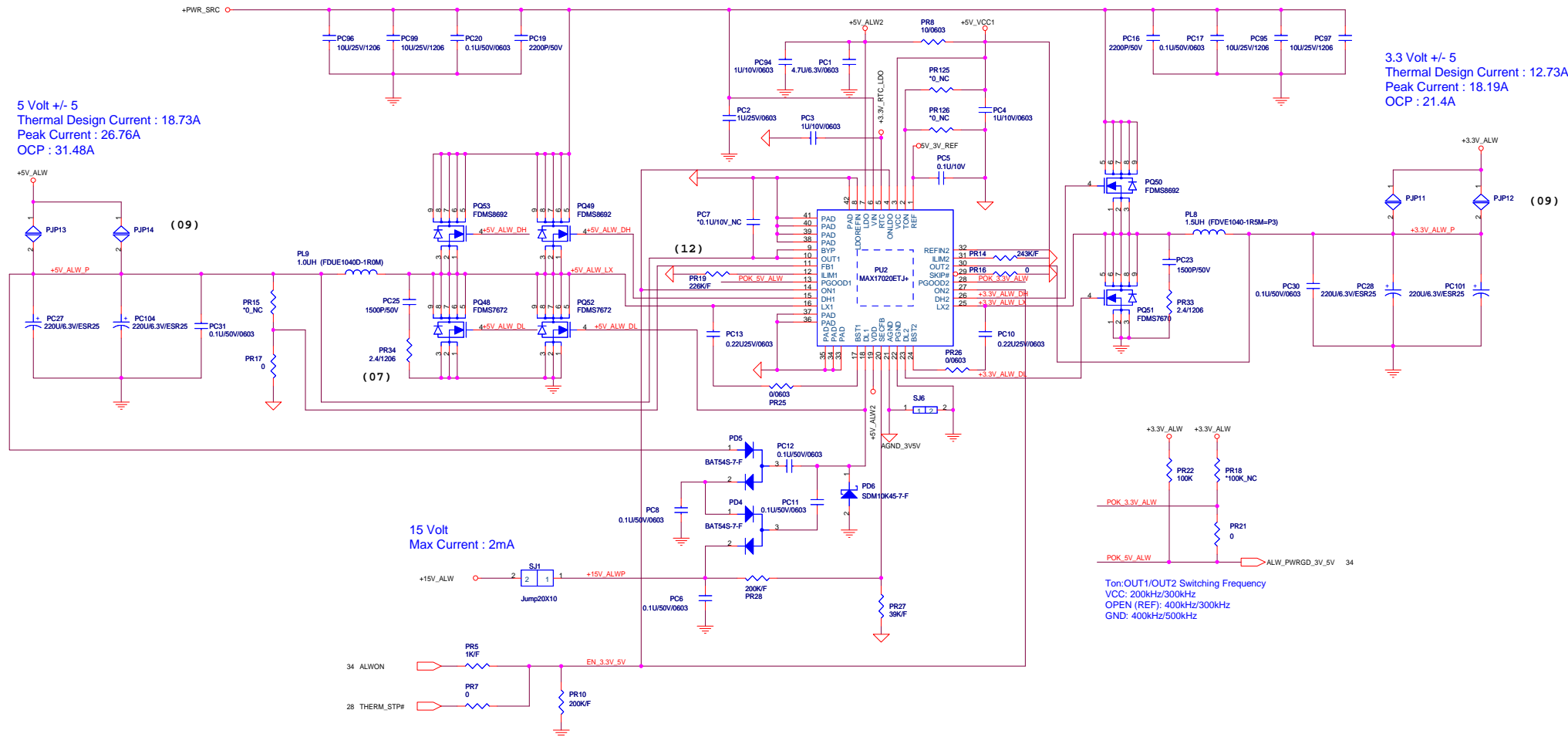


+3.3V_ALW & +5V_ALW & +15V_ALW (MAX17020ETJ+)

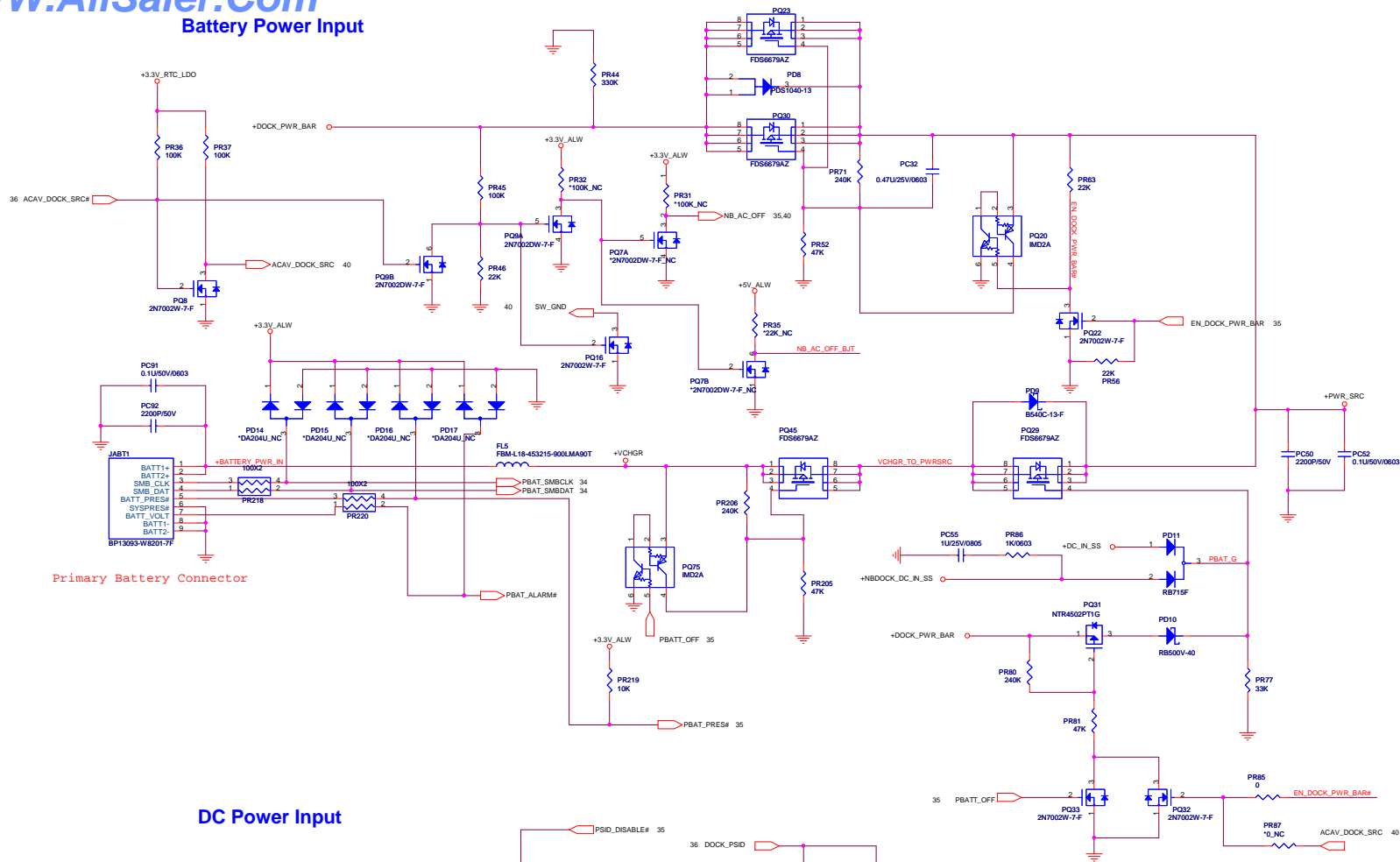
5 Volt +/- 5
Thermal Design Current : 18.73A
Peak Current : 26.76A
OCP : 31.48A

3.3 Volt +/- 5
Thermal Design Current : 12.73A
Peak Current : 18.19A
OCP : 21.4A

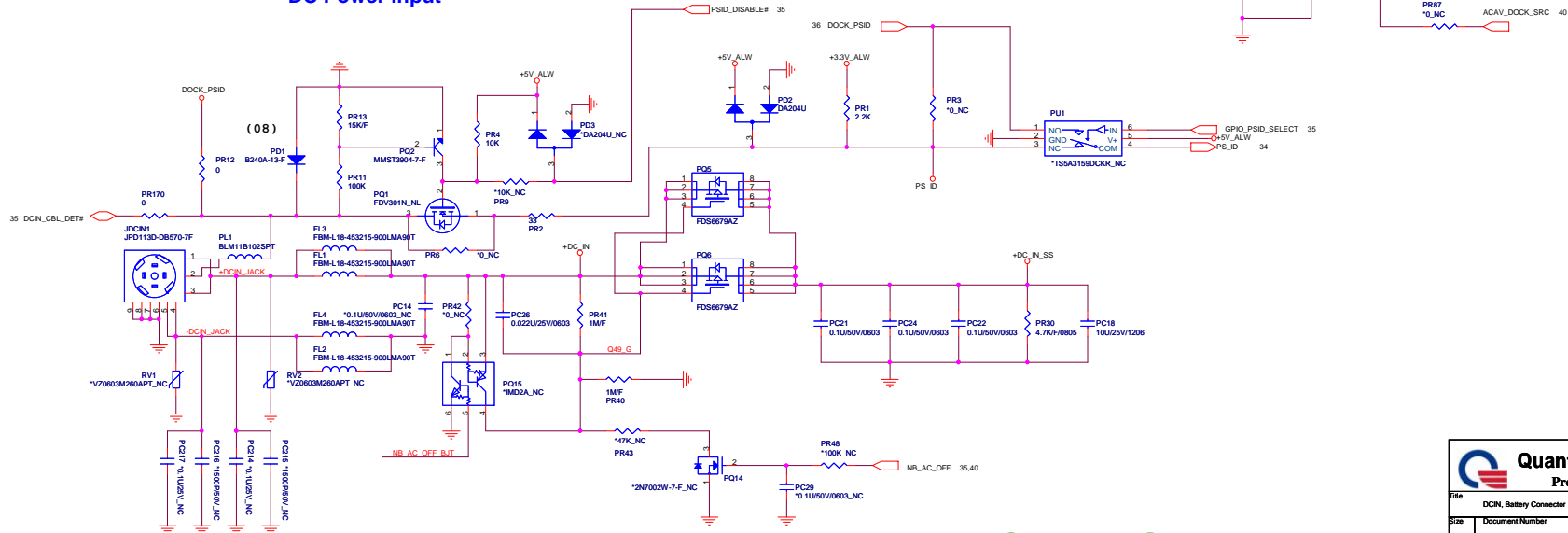
15 Volt
Max Current : 2mA

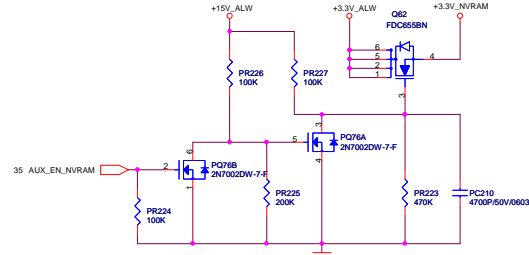
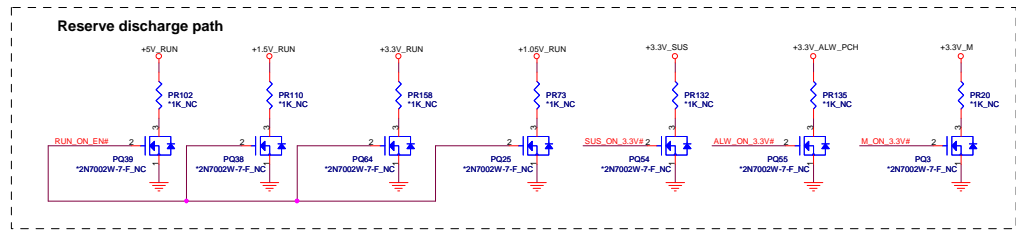
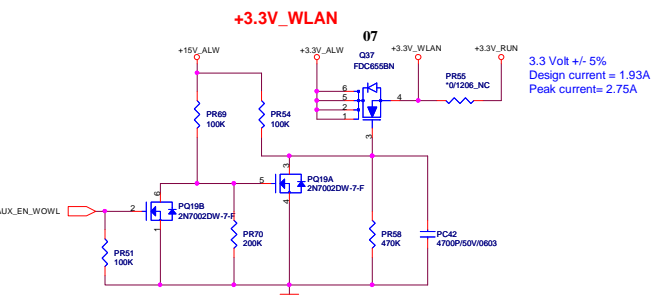
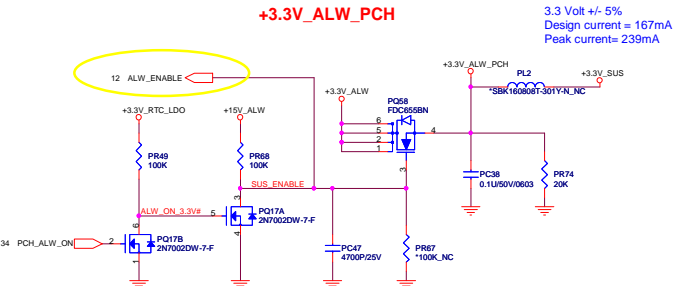
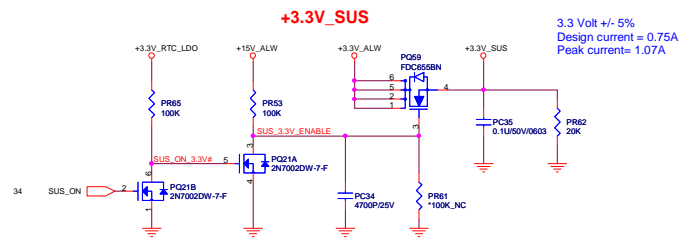
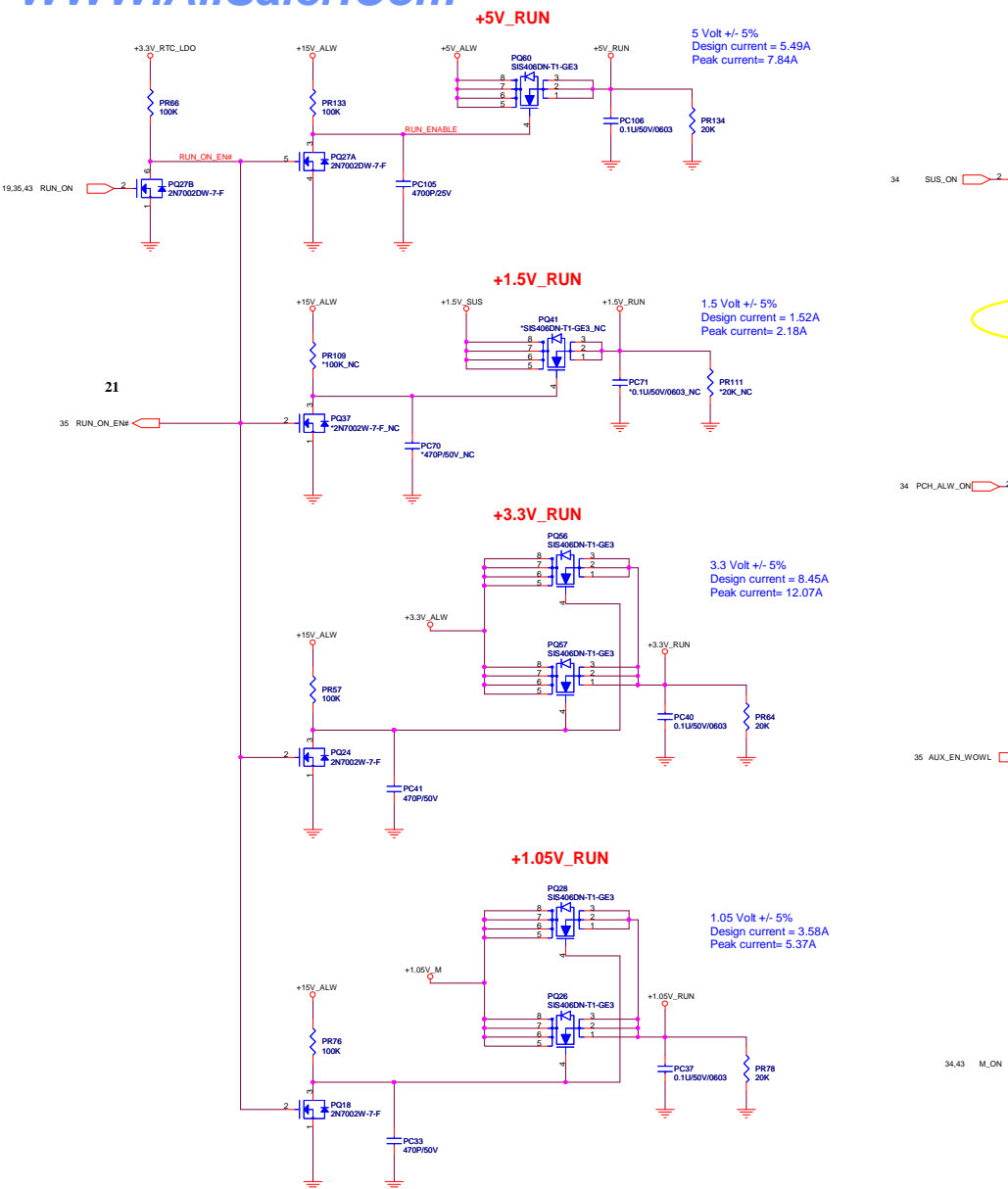


Ton:OUT1/OUT2 Switching Frequency
VCC: 200kHz/300kHz
OPEN (REF): 400kHz/300kHz
GND: 400kHz/500kHz



DC Power Input





Power Mac		Rev E
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